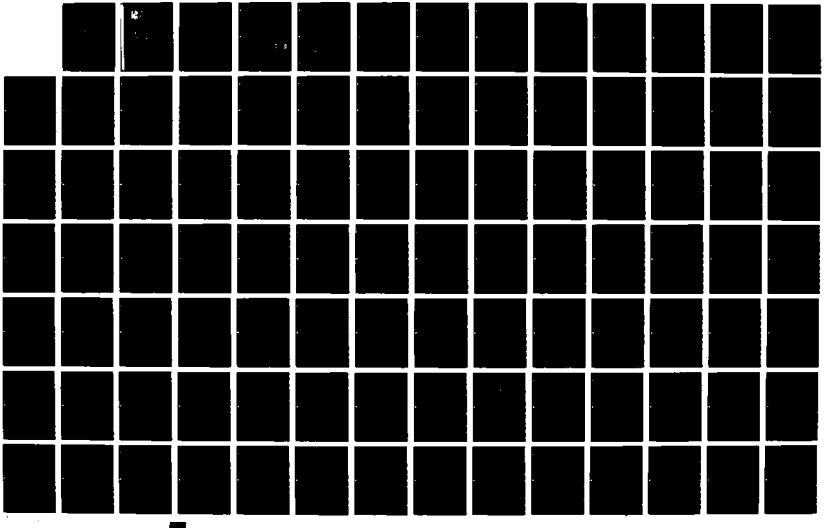
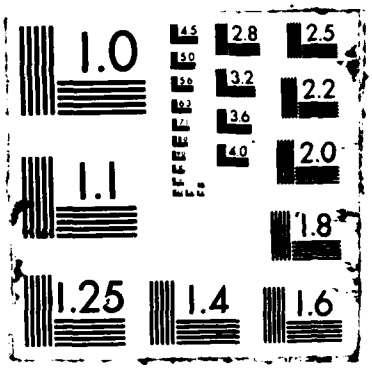
AD-A184 906 ELECTROMAGNETICS AND ELECTROTHERMAL APPROACH TO EVALUATE FAILURES IN MICR..(U) RIT RESEARCH CORP ROCHESTER NY P S NEELAKANTASWAMY AUG 87 RITRC-014

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FINAL REPORT

ONR Contract
N00014-84-K-0532
Project # 613-005
Dr. P.S. Neelakantaswamy
(Principal Investigator)

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RIT RESEARCH CORPORATION
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3. RECIPIENT'S CATALOG NUMBER:	
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7. AUTHOR(s): Dr. P.S. Neelakantaswamy (Principal Investigator)	8. CONTRACT OR GRANT NUMBER(s): N00014-84-K-05
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18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Electrostatic Discharge (ESD), Electrical Overstressing (EOS), Microelectronic Device Reliability

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This Final Report summarizes the following research efforts addressed in the Project: Interaction of electromagnetic overstresses, such as electrostatic discharge (ESD) with the microelectronic devices, resulting IC damage(s) and methods of preventing the related failures.

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ELECTROMAGNETICS AND ELECTROTHERMAL APPROACH TO EVALUATE FAILURES IN MICROELECTRONIC DEVICES CAUSED BY ELECTROSTATIC DISCHARGES: STOCHASTICAL ASPECTS OF THE DEVICE RELIABILITY

Reference:

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FINAL REPORT

A. Introduction

As the conclusion of the contract efforts, this Final Report summarizes the objectives of the studies undertaken, results and conclusions of the research tasks envisaged and the scope for future investigations to be followed.

The objectives of this fundamental research address the following three major efforts:

1. Studies on the interaction of electromagnetics due to electrical overstressing/electrostatic discharge with the microelectronic devices.

2. Evaluation of the resulting susceptibility of devices to damages in terms of cause-effect relations predicting the IC reliability vis-a-vis EOS/ESD.

3. Development of new failure preventive methods/on chip-protection circuits.

The background details which motivated the research impetus are as summarized below:

The damages caused by electrostatic discharges (ESD) seriously challenge the reliability of microelectronic devices since they may result in degraded device performances, system software errors or catastrophic failures. Different technologies present different susceptibility levels to ESD but none is completely immune to their adverse effects.

As ESD-induced damages have been observed even on the early small-scale ICs, efforts have been undertaken to improve the reliability of IC regarding ESD. Although progress was made in the development of electrostatic discharge models and in the design of protective circuits for a few special devices, the threat of ESD considerably increased with the introduction of VLSI/ULSI implementation. The seriousness of the ESD challenge could be better understood by considering the following facts:

1. The device scaling-down to micron or sub-micron level have made microelectronics vulnerable to energies as low as microjoules.

2. The thin gate-oxides which have a thickness of the order of hundred of angstroms can irreversibly be damaged by voltages as low as tens of volts.

3. During ESD, there is a localized power dissipation which is relatively high enough to short circuit the shallow junctions of contemporary devices by forming metal spikes and excessive alloy.

4. Often conductive runners of relatively small cross-sections are destroyed by the transient large current densities produced by ESD, and so on.

In addition to the problems directly associated with the scaling-down in device dimensions, there are thermal problems. In technologies, such as silicon on sapphire (SOS) and silicon on insulator (SOI), the ESD problem is further enhanced due to poor thermal conductivities of sapphire and silicon dioxide. Further microelectronic devices are not free from the susceptibility to damages by ESD even after being installed on a PCB or a subsystem. Likewise, specific studies indicate the existence of failures due to electromagnetic interference (EMI) caused by ESD occurring in proximity to a device. Overstressings due to electromagnetic pulsing (EMP) causing deleterious effects on microchips have also been indentified.

Research envisaged in the Project concerned with the development of methods to model the static-induced failure-modes by considering the electromagnetics associated with the critical current-voltage relations prevalent in the test microelectronic circuit at the instant (or during) a failure. The failure-mode models so developed would enable identification (and/or isolation) of the failure-prone rogue components (or parts) and determine the rate and the extent of damages incurred so that relevant design improvements or counter-measures can be decided to achieve improved intrinsic reliability of the device concerned.

Specifically, the research addressed a detailed study of the menace of Electrostatic Discharges (ESD), inducing damages in microcircuits which are

capable of destroying totally or degrade the performance of bipolar and unipolar devices. Such damages pose a major problem as it is very hard to identify the sources and paths of the electrostatic discharges which are subtle and difficult to be traced. Further, ESD failures can occur at all stages of handling--from the manufacturing-point to the customer-end. Hence the failure characteristics do not concur with the conventional "bath-tub" description of component failures. However, in general, ESD damages involve those parts associated with handling and packaging practices and therefore certain studies exclusive to these vulnerable parts were undertaken.

Inasmuch as ESD failures result from electric transients phenomena, relevant analysis/studies are built-up on time-dependent electromagnetic considerations; the random nature of electric discharge of failure-inducing paths are studied via stochastical aspects. Apart from computer-based simulation studies/analytical failure models, relevant high-voltage pulse-testing were also carried out on devices to trace the hazardous paths involved in the transient electrical conduction within the device infrastructure.

On the basis of the overall results of the studies, suggestions for proper isolation, grounding, encapsulation, handling and packaging of microelectronic devices under various environmental conditions are stipulated so as to ensure higher reliability of microelectronic products.

B. Specific Research Tasks:

I. Theoretical Work

a. EOS/ESD: Electromagnetic Phenomena:

The transient influence of any electrical overstressing (such as electrostatic discharge, ESD) on microelectronic devices are regarded as the time-dependent electromagnetic phenomena which transfer energy from static potential (or from any electrical overstressing source) to the device.

Such transfer of energy has been observed to manifest in two possible modes, namely: 1) direct or invasive influence in which the device in question comes in contact with the overstressing source; and 2) indirect or noninvasive mode wherein the coupling is caused via electromagnetic wave phenomena.

In either case, considering the high magnitude of overstressing voltage which is discharged through a device within nanosecond time-regimes, the proneness of the device to failure would be very high. Hence, in the present research, the following theoretical efforts were considered:

1. Development of theoretical models depicting the realistic electromagnetic transfer of energy in the overstressing transients.

2. Quantification of the resulting formation of electrothermal stresses and other degradation mechanisms in the microelectronic devices.

By these models, the severity levels of ESD/EOS zaps and the corresponding lethality endurance sustained by the semiconductor devices were evaluated. The corresponding results would lead to locating and identifying the maximum ESD-prone regions in practical IC devices which would eventually help in understanding the fundamentals of device survivability under electrical overstressings.

Discrete devices, high density microelectronic devices and other special semiconductor devices such as IMPATT diodes, which are likely to be overstressed, not only due to ESD, but also due to EMP (NEMP, for example) phenomena in military applications, have also been investigated.

Specific attention was paid to consider the areas in which fundamental researching had been lacking. For example, latent failures due to (EMP/EMI-based) noninvasive influence of ESD, transient (overstress-induced) electromagnetic interaction with PCB-mounted and/or hybrids, electromagnetic (transient)

interaction with submicron devices, thermoelastic stressings in the device due to transient EMP/EOS effects, etc., would require considerable research-input and hence were considered in detail.

b. Device-modeling under electromagnetic overstressing:

1. Both bipolar and unipolar devices with shrinking geometries were modeled via rigorous analytical/ numerical methods, to understand their response under electromagnetic overstressings.

2. Device protection circuits were considered in terms of their viability to withstand the electromagnetic overstressings. Relevant changes have been suggested.

II. Experimental Work

To verify the various cause-effect relations pertaining to electromagnetic stressings, some basic tests to simulate the overstressings and to quantify their effects on the devices (such as MOS capacitors, etc.) were conducted. The overall strategy of the research envisaged is summarized in the accompanying flow-chart.

C. Details on the Accomplishments:

Apropos of the specific objectives of the project, the following are the details of the tasks accomplished.

1. Procurement of Documents/Reports and Publications:

--Completed--

2. Dialogue with Industries: Contacts were made with scientists/ engineers dealing with ESD/EOS problems in industries and in laboratories. Valuable exchange of scientific information was carried out and utilized in the investigations.

3. Procurement of Test Instruments and Setting Up of the Laboratory:

--Completed--

4. Research Tasks Completed:

I. Modeling of EOS/ESD as Electromagnetic transient overstressing phenomena.

1. Invasive and noninvasive influences of EOS were distinguished in respect of the following and relevant modelings were done:

a. Direct/Indirect electromagnetic coupling with discrete (large-sized) devices.

b. Direct/Indirect electromagnetic interaction with devices of micron/submicron dimensions.

c. Direct/Indirect coupling of EMP with PCB-mounted and/or hybrid devices.

d. EMP interaction on devices housed inside the equipment: EOS treated as a lethal EMI.

II. Failure/Susceptibility Analyses

a. Concept definitions and quantifications of cause-effect relations relevant to ESD-to-device interaction were developed. They are termed as the Severity Factor and Lethality Endurance Coefficient. These quantities are analytically linked to the Life-Time of the device.

b. Latent failures in the devices resulting from ESD were considered as thermoelastic stress-induced overstresses. Relevant thermodynamical and thermoelastic analyses have been completed.

c. Considering filamentary type of "hot-spot" resulting from electrical transients (such as ESD), the conventional Wunsch-Bell model was modified by a more comprehensive computer-aided algorithm. The method was applied to study IMPATT diode reliability.

d. Thermoelastic-based stress-relief in microelectronic devices was analyzed via crack-propagation principles.

e. Susceptibility aspects of PCB-mounted devices were analyzed.

f. Susceptibility aspects of protective-circuits were evaluated.

g. An EMI model has been developed to assess the non-invasive influence of the ESD on an equipment-mounted device.

h. Assessment of MOS device degradation via noise characteristics was investigated.

i. One-to-one correlation between electrical overstressing and ionizing radiation effects in MOSFETs was elucidated.

j. Susceptibility studies on Stripline-Opposed-Emitter (SOE) package Bipolar Devices have been performed.

III. Protection Circuits and Preventive Studies

a. A comparative study on the relative protection capabilities of all the existing protection circuits was carried out. The survey indicated that the existing protection circuits themselves are prone to damages due to ESD and hence need improvement.

To achieve this, a "junctionless" protective device has been developed on the basis of a geometry using Static Induction Transistor principle.

b. Regarding static conductive materials, relevant design formulations have been developed on the basis of stochastical mixture theory. Such composites are useful as bonding agents in ICs with optimal electrothermal characteristics.

IV. MOS Gate-Oxide Degradation

Considering the possibilities of charges being pumped into the gate-dielectric as a result of external electromagnetic influence, studies to quantify the extent of severity and the amount of charge pumped in and getting trapped in the gate oxide was performed. The effects of trapped charges were being studied in terms of degraded dielectric behavior of the oxide manifesting as 1) reduced break-down strength; 2) non-linear transfer function (g_m) relations; and 3) as increased noise effects.

The state of charge and field distribution in a MOS structure which may arise due to external electromagnetic coupling was also studied exclusively via appropriate modeling of potential distribution in the device (static and transient) in terms of two-dimensional Poisson's equation. Effects of doping level(s)

and channel length have been considered. A formal solution of two-dimensional Poisson's equation by Method of Moments was obtained.

Dielectric degradation was analyzed in terms of low frequency noise performance of the device. Cumulative increase in the noise resistance of the device was quantified in terms of charge injection and trapping resulting from repetitive electromagnetic influence.

Studies pertaining to the analogous influence of ionizing radiations and electrical overstressings on MOS devices were carried out. The resulting damage characteristics were modeled via noise parameters.

It is also investigated to ascertain the extent to which a radiation-hardened device would be tolerant/less-susceptible to electrical overstresses.

D. Research papers and/or reports published or under publication, presented in symposia or under preparation are as follows:

I. Susceptibility Analysis:

1. P.S. Neelakantaswamy, T.K. Sarkar, and R.I. Turkman: Residual Fatigues in Microelectronic Devices Due to Thermoelastic Strains Caused by Repetitive Electrical Overstress: A Model for Latent

Failures. Presented in 7th Annual EOS/ESD Symp., September 1985, Minneapolis, Minnesota.

2. P.S. Neelakantaswamy, R.I. Turkman, and T.K. Sarkar: Filamentary Hot-Spots in Microwave IMPATT Diodes: Modified Wunsch-Bell Model. Presented in 7th Annual EOS/ESD Symp., September 1985, Minneapolis, Minnesota.

3. P.S. Neelakantaswamy, T.K. Sarkar, and R.I. Turkman: On the Threat to Dielectric-Based Devices and Components from Repetitive Nonsinusoidal Electrical Overstresses. Presented in 17th Electrical & Electrical Insulation Conference, September/October 1985, Boston, Massachusetts.

4. P.S. Neelakantaswamy, R.I. Turkman, and T.K. Sarkar: Failures in Microelectronic Devices Due to Thermoelastic Strains Caused by Electrical Overstressings. Presented in 6th Biennial Conference on Failure Prevention and Reliability, September 1985, Cincinnati, Ohio.

5. P.S. Neelakantaswamy, T.K. Sarkar, and R.I. Turkman: Susceptibility of PCB-Mounted Microelectronic Devices to Failures Caused by Electrostatic Discharges. Electronic Packaging & Production, 132-134, February 1987.

6. P.S. Neelakantaswamy, R.I. Turkman, and T.K. Sarkar: Susceptibility of On-Chip Protection Circuits to Latent Failures Caused by

Electrostatic Discharges. Solid State Electronics, Vol. 29 (6), 677-679, 1986.

7. P.S. Neelakantaswamy: Impulsive EMI Radiated by Electrostatic Discharges (ESD). Interference Technology Engineer's Master, 1987 (under Print).

II. ESD Preventive Methods:

1. P.S. Neelakantaswamy and R.I. Turkman: Electrostatic Propensity of Filler-Added Plastics Used in Microelectronics. Presented in RIT Polymer Symposium, May 9, 1986, Rochester, NY.

2. P.S. Neelakantaswamy, R.I. Turkman, and T.K. Sarkar: Complex Permittivity of a Dielectric-Mixture Corrected Version of Lichtenecker's Logarithmic Law of Mixing. Electronics Letters, Vol. 21(7), March 1985, pp. 270-271.

III. Mos Gate-Oxide Degradation:

1. P.S. Neelakantaswamy and R.I. Turkman: Gate-Insulation Degradation in MOS-Devices due to Electrical Overstressings: Characterization via Noise Performance Studies. Presented in 1986 IEEE International Symp. on Electrical Insulation, Washington, D.C., June 8-11, 1986.

2. P.S. Neelakantaswamy and R.I. Turkman: MOS Scaling Effects on ESD-Based Failures. Presented in Custom Integrated Circuit Conference, May 12-15, 1986, Rochester, NY.

3. P.S. Neelakantaswamy and R.I. Turkman: Analogous Influence of Ionizing Radiations and Electrical Overstressings: Damage Characterization via Noise Parameters. Natural Space Radiation and VLSI Technology Conference, Houston, Texas, January 20-21, 1987.

4. P.S. Neelakantaswamy and R.I.Turkman: Noise Characteristics of Ionizing-Radiation Stressed MOSFET Devices. Solid State Electronics (under print).

D. MOS Device Modeling:

1. E. Arvas, R.I. Turkman and P.S. Neelakantaswamy: MOSFET Analysis Through Numerical Solution of Poisson's Equation by Method of Moments. Solid State Electronics (Under Print).

E. Scope for Future Studies/Extended Efforts

The results of the investigations are documented in Technical Reports listed in the Appendix I.

The concepts of the basic research undertaken here have been published (are being published) in refereed journals and/or presented in international symposia. On the basis of feedback received from the scientific and

industrial community, the potential to extend the present studies is excellent.

The scope of the extended tasks beyond the present contract period and the good reasons and the need for such efforts are described in the enclosed Proposal for Continuation of Efforts on the Project #613-005/N00014-84-K-0532 (1984-1987), entitled "Electromagnetic Radiation Effects on Microelectronic Ensembles: Concept Definition and Analysis of Electromagnetic Overstressings," submitted to ONR on 4-28-87.

A set of Technical Reports as listed in Appendix I is also enclosed.

Electromagnetics and Electrothermal Approach to Evaluate Failure in Microelectronic Devices Caused by Electrostatic Discharges: Stochastical Aspects of the Device Reliability

Office of Naval Research Project: N00014-84-K-0532/NR613-005/1984-1987

Principal Investigator: Dr. P.S. Neelakantaswamy

TECHNICAL REPORTS

No.	Title	Authors
1. RITRC 001 Tech Report #01	Solution of Poisson's Equation Using Method of Moments: Application to MOS Devices	E. Arvas P.S. Neelakantaswamy R.I. Turkman
2. RITRC 002 Tech Report #02	ESD/EOS Susceptibility of a Class of Bipolar RF Power Transistor: Experimental Studies on Stripline-Opposed Emitter Transistors	P.S. Neelakantaswamy R.I. Turkman
3. RITRC 003 Tech Report #04	Electrostatic Propensity and Bleed-Off Characteristics of Composite Materials	P.S. Neelakantaswamy R.I. Turkman
4. RITRC 004 Tech Report #04	Filamentary Hot-Spots in Microwave IMPATT Diodes: Modified Wunsch-Bell Model	P.S. Neelakantaswamy R.I. Turkman T.K. Sarkar
5. RITRC 005 Tech Report #05	Failures in Microelectronic Devices due to Thermoelastic Strains Caused by Electrical Overstressings	P.S. Neelakantaswamy R.I. Turkman T.K. Sarkar
6. RITRC 006 Tech Report #06	Susceptibility of On-Chip Protection Circuits to Latent Failures Caused by Electrostatic Discharges	P.S. Neelakantaswamy R.I. Turkman T.K. Sarkar
7. RITRC 007 Tech Report #07	MOS Scaling Effects on ESD-Based Failures	P.S. Neelakantaswamy R.I. Turkman
8. RITRC 008 Tech Report #08	Susceptibility of PCB-Mounted Microelectronic Devices to Failures Caused by Electrostatic Discharges	P.S. Neelakantaswamy
9. RITRC 009 Tech Report #09	Impulsive EMI Radiated by Electrostatic Discharges (ESD)	P.S. Neelakantaswamy
10. RITRC 010 Tech Report #10	Noise Characteristics of MOS Devices Degraded by Electrical Overstressings	P.S. Neelakantaswamy R.I. Turkman
11. RITRC 011 Tech Report #11	Influence of Ionizing Radiations and Electrical Overstressings on MOS Devices: A Comparison	P.S. Neelakantaswamy R.I. Turkman

TECHNICAL REPORTS

(Submitted)

No.	Title	Authors
12. RITRC 012 Tech Report #12	Breakdown in an Electrically Over-stressed Thin Oxide of a MOS Structure: Effects of Field-Plate, Material, Geometry and Perturbations	P.S. Neelakantaswamy R.I. Turkman
13. RITRC 013 Tech Report #13	Studies on On-Chip Protection Circuits: A New Protection Scheme Using Static Induction Transistor Principle	R.I. Turkman P.S. Neelakantaswamy
14. RITRC 014 Tech Report #14	Electromagnetics & Electrothermal Approach to Evaluate Failure in Micro-electronic Devices Caused by Electro-static Discharge (ESD)	P.S. Neelakantaswamy

Research Publications on
Electrical Overstressings and/or Failure Modeling
of Microelectronic Devices

Dr. Perambur S. Neelakantaswamy

1. P.S. Neelakantaswamy, T.K. Sarkar and R.I. Turkman: Residual Fatigues in Microelectronic Devices Due to Thermoelastic Strains Caused by Repetitive Electrical Overstresses: A Model for Latent Failures. Presented at 7th Annual EOS/ESD Symp., Sept. 1985, Minneapolis, Minnesota. Proc. 1985 EOS/ESD Symp., Vol. EOS-7, 1985, 77-83.

2. P.S. Neelakantaswamy, R.I. Turkman and T.K. Sarkar: Filamentary Hot-Spots in Microwave IMPATT Diodes: Modified Gunsch-Bell Model. Presented at 7th Annual EOS/ESD Symp., Sept. 1985, Minneapolis, Minnesota. Proc. 1985 EOS/ESD Symp., Vol. EOS-7, 1985, 92-99.

3. P.S. Neelakantaswamy, T.K. Sarkar and R.I. Turkman: On the Threat to Dielectric-Based Devices and Components from Repetitive Non-Sinusoidal Electrical Overstresses. Presented at 17th Electrical & Electrical Insulation Conference, Sept./Oct. 1985, Boston, Massachusetts. Proc. 17th E/EI Conf., 1985, 350-354.

4. P.S. Neelakantaswamy, R.I. Turkman and T.K. Sarkar: Failures in Microelectronic Devices Due to Thermoelastic Strains Caused by Electrical Overstressings. Presented at 6th Biennial Conference on Failure Prevention and Reliability, September 1985, Cincinnati, Ohio. ASME Bound Vol. H00333, 1-5.

5. P.S. Neelakantaswamy and R.I. Turkman: MOS Scaling Effects on ESD-Based Failures. Presented at IEEE Custom Integrated Circuits Conference, May 12, 1986, Rochester, NY. Proc. 1986 IEEE CIC Conf., 400-403.

6. P.S. Neelakantaswamy and R.I. Turkman: Noise Performance Studies to Assess MOS-Degradation Due to Impulsive Overstresses. Presented at 4th International Microelectronics Conference, May 20-30, 1986, Kobe, Tokyo.

7. P.S. Neelakantaswamy, R.I. Turkman and T.K. Sarkar: Susceptibility of On-Chip Protection Circuits to Latent Failures Caused by Electrostatic Discharges. Solid State Electronics (U.K.), Vol. 29(6), 1986, 677-679.

8. P.S. Neelakantaswamy and R.I. Turkman: Gate Insulator Degradation in MOS-Devices Due to Electrical Overstresses. Characterization via Noise Performance Studies. Presented at 1986 IEEE International Symp. on Electrical Insulation, June 8-11, 1986, Washington, D.C., (Proc. 1986 IEEE Intl. Symp. on EI, 327-330).

9. P.S. Neelakantaswamy: Impulsive EMI Radiated by Electrostatic Discharges (ESD). Interference Technology Engineer's Master 1987 (U.S.A), 104-110.

10. P.S. Neelakantaswamy and R.I. Turkman: Analogous Influence of Ionizing Radiations and Electrical Overstressings: Damage Characterization via Noise Parameters. Presented at Natural Space Radiation & VLSI Technology Conf., Jan. 1987, Johnson Space Center, NASA, Houston, Texas.

11. P.S. Neelakantaswamy and R.I. Turkman: Susceptibility of PCB-Mounted Microelectronic Devices to Failures Caused by Electrostatic Discharges. Electronic Packaging & Production (U.S.A.), February 1987, 132-134.

12. P.S. Neelakantaswamy and R.I. Turkman: Noise Characteristics of Ionizing-Radiation Stressed MOSFET Devices. Solid State Electronics (U.K.), (Under Print).

13. E. Arvas, R.I. Turkman and P.S. Neelakantaswamy: MOSFET Analysis Through Numerical Solution of Poisson's Equation by Method of Moments. Solid State Electronics (U.K.), (Under Print).

14. P.S. Neelakantaswamy and R.I. Turkman: ESD/EOS Susceptibility of Strip-Line-Opposed Emitter Transistors. Evaluation Engineering (U.S.A.), (To Appear in July 1987 Issue).

15. P.S. Neelakantaswamy and R.I. Turkman: Voltage Breakdown in MOS Capacitors: Overstressing Severity due to the Geometry and Material of the Field Plate. Solid State Electronics (U.K.), (Under Review).

16. R.I. Turkman and P.S. Neelakantaswamy: A Novel On-Chip ESD Protection Device Using Static Induction Transistor Principle. Paper to be presented in 9th Annual EOS/ESD Symp., Sept. 29-Oct. 1, 1987, Orlando, Florida.

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REPORT DOCUMENTATION PAGE

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	6. PERFORMING ORG. REPORT NUMBER
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9. PERFORMING ORGANIZATION NAME AND ADDRESS: RIT Research Corporation, 75 Highpower Road, Rochester, NY 14623-3435	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: NR 613-005
11. CONTROLLING OFFICE NAME AND ADDRESS: Department of Navy, Office of Naval Research, Arlington, VA 22217	12. REPORT DATE: March 1986
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18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

MOS DEVICES, POISSON'S EQUATION (TWO-DIMENSIONAL), METHOD OF MOMENTS,

THRESHOLD VOLTAGE, SURFACE POTENTIAL

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

An algorithm for the computation of solution to Poisson's equation in a two-dimensional domain is developed in terms of equivalent sources on the boundary. The region considered can be of arbitrary shape, and the boundary conditions can be Dirichlet, Neumann or mixed type. The solution is obtained by method of moments. Pulse expansion and point matching techniques are used. Computed results closely agree with the available data concerning MOS devices.

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SOLUTION OF POISSON'S EQUATION USING METHOD OF MOMENTS: APPLICATION TO MOS DEVICES

by

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CONTENTS

	Page
ABSTRACT	1
I. INTRODUCTION	2
II. STATEMENT	3
III. METHOD OF SOLUTION	3
IV. SAMPLE RESULTS	4
V. APPLICATION TO MOS STRUCTURES	5
VI. REFERENCES	6
APPENDIX A: COMPUTER PROGRAM	8
PROGRAM LISTING	11
SAMPLE INPUT/OUTPUT FILE	23
FIGURES 1 - 8	26

ABSTRACT

An algorithm for the computation of solution to Poisson's equation in a two-dimensional domain is developed in terms of equivalent sources on the boundary. The region considered can be of arbitrary shape, and the boundary conditions can be Dirichlet, Neumann or mixed type. The solution is obtained by method of moments. Pulse expansion and point matching techniques are used. Computed results closely agree with the available data concerning MOS devices.

I. INTRODUCTION

Poisson's equation is one of the most important differential equations of physics. For example, it can be used to find the threshold voltages of MOSFET's. When the channel length is small, the depletion-layer widths of the source and drain junctions are comparable to the channel length, and the potential distribution is two dimensional amenable for solution via Poisson's equation.

In this work we give a simple method for solving two-dimensional Poisson's equation in a region subject to general boundary conditions on the bounding surface. Equivalent surface charges are placed just outside the boundary and the total potential (produced by the impressed volume charges and the equivalent surface charges) is enforced to satisfy the boundary conditions. This transforms the boundary value problem into an integral equation for the equivalent surface charges. Then the method of moments [1] is used to solve the integral equation numerically.

II. STATEMENT OF PROBLEM

Consider a 2-dimensional region R bounded by the contour C as shown in Figure 1. The problem is to find the total potential ψ (x,y) in R which satisfies the Poisson's equation

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = -\rho_v/\varepsilon \qquad (1)$$

in R, with the boundary condition(s)

$$\alpha\psi + \beta \frac{\partial \psi}{\partial n} = \gamma \qquad (2)$$

on C.

In eqn. (1), ρ_v denote the volume charge density, and ε is the permittivity of the material in R.

In eqn. (2), α , β and γ denotes known functions defined on C.

Note that the general condition of eqn. (2) includes, as special cases, of Dirichlet (α =1, β =o) and Neumann (α =o, β =1) conditions.

The Laplace's equation is the special case of eqn. (1) with ρ_v = o The solution of Laplace's equation is given in detail in [2]. The present work is an extension of the work in [2], modified for Poisson's equation applied to MOS structures.

III. METHOD OF SOLUTION

In solving eqn. (1) subject to boundary condition of eqn. (2) we let

$$\psi = \phi_p + \phi_h \qquad (3)$$

where (4)

$$\nabla^2 \phi_p = \frac{-\rho_v}{\varepsilon} \quad \text{(in R)}$$

and (5)

$$\nabla^2 \phi_h = 0 \quad \text{(in R)}$$

The solution to eqn. (4) is

$$\phi_p = \frac{1}{2\pi\epsilon} \iint_R \rho(\underline{r}') \ln \frac{k}{\underline{r} - \underline{r}'} \, dx'dy' \tag{6}$$

where $\underline{r}$ and $\underline{r}'$ denote the radius vector to the field and a source point respectively, $\rho(\underline{r}')$ is the value of the impressed charged density at $\underline{r}'$s and k is an arbitrary constant (taken as 100.0 in this work).

The Laplacian potential ϕ_h can be assumed to be produced by some equivalent surface charges, σ , outside R (Fig. 2). Hence ϕ_h is the solution of eqn. (5) subject to boundary condition

$$\alpha\phi_h + \beta \frac{\partial\phi_h}{\partial n} = \gamma - \alpha\phi_p - \beta \frac{\partial\phi_p}{\partial n} \quad \text{on C} \tag{7}$$

Since ϕ_h has the form

$$\phi_h = \frac{1}{2\pi\epsilon} \iint_C \sigma \ln \frac{k}{\underline{r} - \underline{r}'} \, dx'dy' \tag{8}$$

we see that eqn. (7) is an integral equation for σ .

Note that (5) subject to the boundary condition of eqn. (7) is the same boundary value problem as the one considered in [2]. We use pulse expansion and point-matching techniques to solve this problem.

The approach involved is to first model the surface C by N planar strips and the assume a constant charge density on each segment. Satisfying the boundary condition of eqn. (7) at the center of each of N strips, gives N algebraic equations. The solution of these equations gives the value of the constant charge density on each strip. The details are elaborated in [2]. Once eqn. (7) is solved for σ , we obtain the total potential ψ using eqns. (8), (6) and (3).

IV. SAMPLE RESULTS

A FORTRAN program is written to implement the theory developed above.

The first test problem that we tried is shown in Fig. 3, where a line charge of $\rho_1 = 8.854 \times 10^{-12}$ C/m is placed at the center of a grounded rectangular boundary. The total potential was evaluated at the points A, B, C and D as shown.

Table 1 illustrates the convergence of the computed results as the number N of segments is increased. The exact result [3, eqn. 4-7.23] is also shown for comparison. The last column of the table shows the CPU time on a VAX 11/782.

A second test problem formulated to study a short channel MOSFET is described hereunder.

VI. APPLICATION TO MOS STRUCTURES

To demonstrate the applicability of the proposed numerical method to MOS structures, a test N-channel MOSFET illustrated in Fig. 4 is considered. The rectangular depletion region under the gate and its expanded view with the relevant boundary conditions are depicted in Fig. 5.

The notations followed are those detailed in [4]. Figs. 6 and 7 illustrate the surface potential Ψ (x, y = d) variation along the channel for 2 typical devices with channel lengths L = 1 μ m and 5 μ m respectively.

The corresponding threshold voltage $(V_T - V_{FB})$ versus channel length for drain voltage (V_D) of 0 and 5V is presented in Fig. 8.

For comparison, along with the computed data, the results obtained by (approximate) closed-form solution due to Poole and Kwong [4] are also shown in Figs. 6, 7 and 8.

Referring to these figures (Figs. 6, 7 and 8), close agreement between the results may be observed. Any deviation can be attributed to the approximations involved in the truncation of the series solution given in [4] and due to the variations in the values of d and V_{gm} considered in the analysis.

However, the present work indicates the applicability of the method of solution envisaged to the MOS structures. This method can be extended to a more realistic model of the MOS structure involving curved depletion boundaries and the depletion width (d) varying along the channel length.

Further, this steady state solution can be extended to study transient causes pertaining to ESD/EOS induced effects.

V. REFERENCES

[1] R. F. Harrington, Field Computations by Moment Methods. New York: Macmillan, 1968; reprinted by Krieger, Melbourne, FL, 1982.

[2] R. F. Harrington, K. Pontoppidan, P. Abrahamsen and N. C. Albertsen, "Computation of Lapacian Potentials by an equivalent-source method", Proc. IEE, Vol. 116, No. 10, pp. 1715-1720, Oct. 1969.

[3] S. Seely and A. D. Poularikas, Electromagnetics, Marcel Dekker, Inc., New York, 1979.

[4] D. R. Poole and D. L. Kwong, "Two Dimensional Analytical Modeling of Threshold Voltages of Short-Channel MOSFET's," IEEE Electron Device Letters, Vol. Edl-5, No. 11, pp. 443-448, Nov. 1984.

Table I

Potential computed for the problem of Fig. 3

N	A (0.25,0.75)	B (0.25,0.50)	C (0.1,0.25)	D (0.45,0.95)	CPU Time (Sec.)
4	0.05924	0.1133	0.01411	0.3145	3.28
8	0.07271	0.1268	0.02757	0.3280	3.55
12	0.07113	0.1226	0.02875	0.3244	4.03
16	0.07050	0.1221	0.02747	0.3238	4.54
20	0.07032	0.1219	0.02721	0.0236	5.15
24	0.07024	0.1218	0.02719	0.3235	5.92
32	0.07018	0.1217	0.02714	0.3234	7.86
40	0.07016	0.1217	0.02712	0.3234	10.69
60	0.07014	0.1216	0.02711	0.3234	21.43
80	0.07014	0.1216	0.02711	0.3234	37.59
Exact					

APPENDIX A: COMPUTER PROGRAM

The FORTRAN computer program is composed of a main and 9 subprograms. The subprograms are:

INFOR
SOLTN
VMATRX
ZMATRX
FIELD
ELSV
POTEN
INTG
GRAD

The last three programs compute the potential and its gradient at a point (x,y) due to the impressed charge distribution. Hence, as the source is charged, these programs must be changed accordingly.

The Main Program:

The main program reads in:

a) the number (NTOTAL) of the straight line segments approximately the boundary C of the region R.

b) the dielectric constant (SPSR) of the medium R.

c) the parameter LAPOIS. If LAPOIS is equal to zero, the problem is to solve the Laplace's equation. (In this case the last three subroutines are not needed). If LAPOIS is equal to 1, we are solving Poisson's equation and hence the potential and its gradient produced by the impressed sources must be provided by the last three subroutines.

For each of NTOTAL linear segments, the main program calls the subprogram INFOR. Then it calls the subroutine SOLTN.

The INFOR subprogram:

The subroutine INFOR reads in

a) The coordinates (X1, Y1) and X2, Y2) of the starting and ending points of each linear segment approximating the boundary C. (X1, Y1, X2, Y2 are in micrometers).

b) The number NSEC, of subsections that each linear segment is to be divided into.

c) For each linear segment α , β and σ are read in. These are sent back to the main program, where they are stored in the matrix BCOND.

In the subroutine INFOR, the coordinates of the starting and ending points of each subsection is computed. This information is stored in arrays XV1, YV1, XV2 and

The subroutine SOLTN:

In this subroutine the moment matrix equation is formed and solved. This subroutine calls various subroutines.

i) The subroutine VMATRX:

In this subroutine the right hand side of eqn. (7) is computed at the center of each subsection. The result is stored in the array V.

ii) The subroutine ZMATRX:

In this subroutine the moment matrix Z is computed. The (i,j) th element of this matrix is the right hand side of eqn. (7), computed at the center of jth subsection. (0 here is the potential produced by a constant charge density of $1(C/m^2)$ on the jth subsection).

iii) The subroutine ELSV:

This subroutine takes the inverse of the moment matrix Z and stores the inverse matrix into the Z matrix.

Once Z matrix is inverted, the surface density is computed in SOLTN subroutine by multiplying the inverse of the Z matrix by the column vector V. The charge density is stored in the array I.

iv) The subroutine FIELD:

This subroutine computes the total potential at K points equally spaced between the points. (XIN, YIN) and XFIN, YFIN)

The last three subroutines compute the potential and its gradient at a given point due to a constant volume charge density RHO (C/m^3) in a rectangular cylinder of infinite length.

INPUT/OUTPUT OF THE PROGRAM

The input to the program is through the data file 92. The first line of the input file is

NTOTAL, EPSE, LAPOIS

Then we have NTOTAL pairs of lines which have the form
X1, Y1, X2, Y2, NSEC

ALPHA, BETA, GAMA.

Where (X1, Y1) and (X2, Y2) denote the coordinates of the starting and ending point of a linear segment, and NSEC is the number of subsection, that the segment will be subdivided into ALPHA, BETA AND GAMA show the values of α , β and σ on the segment.

The last line in the input file has the form
XIN, YIN, XFIN, YFIN, K where (X IN, YIN) and (XFIN, YFIN) are the coordinates of two points, and K is an integer. The program will compute the total potential at K equidistant points lying between the points (XIN, YIN) and (XFIN, YFIN).

The output of the program is printed in data file 18. Here the potential at K points is printed. X and Y are the coordinates of the point at which the potential is computed.

PROGRAM LISTING

The following is the listing of the program:

```
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C THIS PROGRAM COMPUTES THE  EQUIVALENT ELECTRIC                        C
C CHARGE DENSITY ON THE SURFACE OF A LOSSLESS DIELECTRIC                C
C CYLINDER. THIS IS A TWO-DIMENSIONAL PROBLEM. THE TOTAL                C
C POTENTIAL INSIDE THE DIELECTRIC IS DUE TO SOME SPECIFIED              C
C CHARGES INSIDE AND DUE TO SOME IMPRESSED POTENTIALS                   C
C ALONG THE SURFACE.                                                    C
C                                                                       C
C AT ANY POINT ON THE BOUNDARY OF THE CYLINDER WE HAVE                  C
C                                                                       C
C ALPA(C)*POT(CHARGE)+BETA(C)*(D/DN)(POT(CHARGE)) = -ALPHA(C)           C
C *POT(SOURCE)-BETA(C)*(D/DN)POT(SOURCE)+GAMA(C)                        C
C                                                                       C
C WHERE;                                                                C
C C SHOWS THE VARIABLE ALONG THE BOUNDARY OF THE CYLINDER,              C
C ALPHA(C), BETA(C) AND GAMA(C) ARE THREE FUNCTIONS THAT ARE            C
C SPECIFIED AT ANY POINT C,                                             C
C POT(CHARGE)=POTENTIAL PRODUCED AT THE POINT C, BY THE                 C
C UNKOWN EQUIVALENT SURFACE CHARGE RESIDING ON THE BOUNDARY             C
C OF THE CYLINDER,                                                      C
C (D/DN) IS AN OPERATOR WHICH GIVES THE NORMAL DERIVATIVE               C
C OF THE FUNCTION THAT IT OPERATES ON , AND                             C
C POT(SOURCE) IS THE POTENTIAL PRODUCED BY THE IMPRESSED                C
C  SOURCES AT THE POINT ON THE BOUNDARY. THE IMPRESSED                  C
C SOURCES ARE THE VOLUME CHARGE DENSITY INSIDE THE CYLINDER.            C
C THESE ARE THE SOURCES THAT APPEAR ON THE RIGHT                        C
C HAND SIDE OF THE POISSON'S EQUATION.                                  C
C                                                                       C
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C
      IMPLICIT COMPLEX*16 (C)
      IMPLICIT REAL*8(A-B,E-H,P-Z)
      DIMENSION  V(200),RI(200),Z(200,200)
      DIMENSION XV1(200),YV1(200),XV2(200),YV2(200)
      COMMON/NNN/NDP(10),BCOND(10,3),NTOTAL
      COMMON/TYPE/LAPOIS,EPSR
      NMAX=200
C
C  READ TOTAL NUMBER  ,NTOTAL,OF LINEAR SEGMENTS WHICH
C  CONSTITUTE THE BOUNDARY FOR THE PROBLEM. ALSO
C  READ THE DIELECTRIC CONSTANT ,EPSR, OF
C  THE MEDIUM.
C
C  IF LAPOIS IS ZERO THEN WE ARE SOLVING LAPLACE EQUATION
C  IF LAPOIS IS ONE THEN THE PROBLEM IS POISSON TYPE.
C
      READ(92,*) NTOTAL,EPSR,LAPOIS
      IF(LAPOIS.EQ.1)WRITE(93,1232)
      IF(LAPOIS.EQ.0)WRITE(93,1233)
 1232 FORMAT(/,25X,'THIS IS POISSON S EQUATION:',/)
 1233 FORMAT(/,25X,'THIS IS LAPLACE S EQUATION:',/)
      WRITE(93,1234)NTOTAL,EPSR
 1234 FORMAT(25X,'-------------------------------------'
     4 ,//,10X,'NO. OF TOTAL LINEAR SEGMENT BOUNDARIES=',I2,/,10X,
     4 'THE DIELECTRIC CONSTANT OF THE CYLINDER IS=',F8.4,//)
      NAI=0
      NBI=0
```

```
C
        DO 199 I=1,NTOTAL
C
C FOR EACH OF NTOTAL LINEAR SEGMENTS FORMING THE BOUNDARY
C CALL THE INFORMATION (INFOR) SUBROUTINE TO  ;
C A) READ IN THE COORDINATES (X1,Y1) OF THE INITIAL POINT AND (X2,Y2)
C    OF THE FINAL POINT OF I'TH LINEAR SEGMENT.
C B) READ IN THE NUMBER ,NSEC, OF SMALLER SUBSECTIONS THAT THIS PARTICULAR
C    LINEAR SEGMENT IS TO BE DIVIDED. THE CENTER OF EACH OF THESE
C    SUBSECTIONS IS A MATCHING POINT.
C C) READ THE VALUES ALPHA, BETA, AND GAMA FOR THIS PARTICULAR
C    LINEAR SEGMENT.
C D) FIND THE COORDINATES OF THE STARTING AND ENDING POINTS OF THESE
C     SUBSECTIONS AND STORE THEM IN THE ARRAYS XV1,YV1,XV2,YV2.
C
C
C
        CALL INFOR(XV1,YV1,XV2,YV2,NAI,NMAX,A,B,G)
        NDP(I)=NAI-NBI
        BCOND(I,1)=A
        BCOND(I,2)=B
        BCOND(I,3)=G
C
C WRITE THE BOUNDARY CONDITIONS DATA FOR THIS LINEAR SEGMENT;
C
        WRITE(93,111)
 111    FORMAT('1')
        WRITE(93,112) I,A,B,G
 112    FORMAT(////5X,'THIS IS THE INFORMATION OF THE
     $  BOUNDARY =',1X,I3,//,5X,'HERE ALPHA=',F9.5,3X,
     $  'BETA=',E11.4,3X,'GAMA=',F9.5,/)
C
C WRITE GEOMETRICAL DATA FOR THIS LINEAR SEGMENT;
C
        WRITE(93,114)
 114    FORMAT(////12X,2('X-COORDINATE',5X,'Y-COORDINATE',5X))
        WRITE(93,115)(J,XV1(J),YV1(J),XV2(J),YV2(J),J=NBI+1,NAI)
 115    FORMAT(//(5X,I3,4(2X,1E))/)
        NBI=NAI
 199    CONTINUE
C
C OBTAIN THE TOTAL NUMBER OF UNKNOWNS IN THE MATRIX EQUATION.
C
        NUNKNS=NAI
        WRITE(93,993)NUNKNS
993     FORMAT(5X,'TOTAL NO. OF UNKNOWNS=',I3,//)
C
C CALL THE SOLUTION SUBROUTINE TO SOLVE THE PROBLEM.
C
        CALL SOLTN(Z,V,RI,XV1,YV1,XV2,YV2,NUNKNS,NMAX)
998     CONTINUE
        STOP
        END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
        SUBROUTINE INFOR(XV1,YV1,XV2,YV2,NAI,NM,A,B,G)
        IMPLICIT COMPLEX*16 (C)
        IMPLICIT REAL*8(A-B,E-H,P-Z)
C
C IN THIS SUBROUTINE THE DATA IS ARRANGED IN THE PROPER FORM
```

```
C FOR FURTHER COMPUTATIONS.
C
      DIMENSION XV1(NM),YV1(NM),XV2(NM),YV2(NM)
      NNODES=NAI
C READ THE COORDINATES (X1,Y1) AND (X2,Y2),
C READ THE NUMBER OF SECTIONS OF THE BOUNDARY (NSEC),
C ALSO READ THE BOUNDARY CONDITIONS INFORMATION; ALPHA(A),
C BETA(B) AND GAMA(G)
C
C
      READ(92,*)X1,Y1,X2,Y2,NSEC
      X1=X1*1.D-06
      Y1=Y1*1.D-06
      X2=X2*1.D-06
      Y2=Y2*1.D-06
      READ(92,*)A,B,G
      EDELX=(X2-X1)/FLOAT(NSEC)
      EDELY=(Y2-Y1)/FLOAT(NSEC)
      DO 20 J=1,NSEC
      NNODES=NNODES+1
      XV1(NNODES)=X1+FLOAT(J-1)*EDELX
      YV1(NNODES)=Y1+FLOAT(J-1)*EDELY
 20   CONTINUE
      DO 70 I=NAI+1,NNODES-1
      XV2(I)=XV1(I+1)
      YV2(I)=YV1(I+1)
 70   CONTINUE
 75   XV2(NNODES)=X2
      YV2(NNODES)=Y2
 76   NAI=NNODES
      RETURN
      END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      SUBROUTINE SOLTN(Z,V,RI,XV1,YV1,XV2,YV2,N,NM)
C
C IN THIS SUBROUTINE THE MATRIX EQUATION AX=Y IS SOLVED USING THE
C METHOD OF MOMENTS.
C
      IMPLICIT COMPLEX*16 (C)
        IMPLICIT REAL*8(A-B,E-H,P-Z)
      DIMENSION V(N),RI(N),Z(N,N),AUX1(600),AUX2(600)
      DIMENSION XV1(NM),YV1(NM),XV2(NM),YV2(NM)
      COMMON/NNN/NDP(10),BCOND(10,3),NTOTAL
C
C INTIALIZE THE VECTORS Z,V,AND RI.
C
      DO 5 I=1,N
      V(I)=0.D0
      RI(I)=0.D0
 5    CONTINUE
      DO 10 I=1,N
      DO 10 J=1,N
      Z(I,J)=0.D0
 10   CONTINUE
C
C CALL THE SUBROUTINE VMATRX TO COMPUTE THE EXCITATION VECTOR.
C
      CALL VMATRX(V,N,XV1,YV1,XV2,YV2,NM)
C
```

```
C CALL THE ZMATRX SUBROUTINE TO OBTAIN THE IMPEDANCE MATRIX.
C
      CALL ZMATRX(Z,XV1,YV1,XV2,YV2,N,NM)
C
C CALL THE ELSV SUBROUTINE TO INVERT THE MATRIX.
C
      EP=0.1D-09
      CALL ELSV(Z,AUX1,AUX2,N,DE,EP)
      WRITE(93,118)DE
 118  FORMAT(5X,'DE =',1E)
C
C MULTIPLY THE INVERSE OF Z-MATRIX WITH THE EXCITATION VECTOR
C TO OBTAIN THE CHARGES.
C
      DO 25 I=1,N
      SUM=0.D0
      DO 24 J=1,N
      SUM=SUM+Z(I,J)*V(J)
 24   CONTINUE
      RI(I)=SUM
 25   CONTINUE
C
C WRITE THE CHARGES ON THE OUTPUT FILE.
C
      NF=0
      DO 135 JKLM=1,NTOTAL
      NI=NF+1
      NF=NF+NDP(JKLM)
      WRITE(93,101)
 101  FORMAT('1')
      WRITE(93,102) JKLM
 102  FORMAT(//5X,'CHARGES ON THE  BOUND. =',1X,I2,//)
        ALPHA=BCOND(JKLM,1)
        BETA=BCOND(JKLM,2)
        GAMA=BCOND(JKLM,3)
        WRITE(93,198)ALPHA,BETA,GAMA
198     FORMAT(5X,'FOR THIS BOUNDARY    ALPHA=',E11.4,
     &3X,'BETA=',E11.4,3X,'GAMA=',E11.4,//)
      DO 30 I=NI,NF
      WRITE(93,105) I,RI(I)
 105  FORMAT(/1X,I3,5X,E11.4)
 30   CONTINUE
135     CONTINUE
        CALL FIELD(RI,N,XV1,XV2,YV1,YV2,NM)
        RETURN
      END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      SUBROUTINE VMATRX(V,N,XV1,YV1,XV2,YV2,NM)
C
C IN THIS SUBROUTINE THE EXCITATION VECTOR V IS
C COMPUTED .
C
      IMPLICIT COMPLEX*16 (C)
        IMPLICIT REAL*8(A-B,E-H,P-Z)
      DIMENSION V(N),XV1(NM),YV1(NM),XV2(NM),YV2(NM)
        COMMON/NNN/NDP(10),BCOND(10,3),NTOTAL
        COMMON/TYPE/LAPOIS,EPSR
        PI=4.D0*DATAN(1.D0)
        TP=2.D0*PI
        EPS=EPSR*8.854D-12
```

```
      IF(LAPOIS.EQ.1)TP=TP-EPS
      NF=0
      DO 110 JKLMN=1,NTOTAL
      NI=NF+1
      NF=NF+NDP(JKLMN)
      ALPHA=BCOND(JKLMN,1)
      BETA=BCOND(JKLMN,2)
      GAMA=BCOND(JKLMN,3)
      DO 100 I=NI,NF
      V(I)=GAMA*TP
      IF(LAPOIS.EQ.0)GO TO 100
      X1=XV1(I)
      Y1=YV1(I)
      X2=XV2(I)
      Y2=YV2(I)
      XF=(X1+X2)/2.0
      YF=(Y1+Y2)/2.0
      IF(ALPHA.EQ.0.0)GO TO 90
      CALL POTEN(XF,YF,POT)
      V(I)=V(I)-ALPHA*POT
C     IF(LAPOIS.EQ.1.AND.BETA.EQ.0.0)V(I)=10.0*V(I)
      IF(BETA.EQ.0.0)GO TO 100
 90   CALL GRAD(XF,YF,POTX,POTY)
      FNRMD=-(X2-X1)*POTY
      FNRMD=FNRMD+(Y2-Y1)*POTX
      FL=SQRT((X2-X1)*(X2-X1)+(Y2-Y1)*(Y2-Y1))
      V(I)=V(I)-BETA*FNRMD/FL
 100  CONTINUE
 110  CONTINUE
      RETURN
      END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      SUBROUTINE ZMATRX(Z,XV1,YV1,XV2,YV2,N,NM)
C
C IN THIS SUBROUTINE THE Z-MATRIX IS FORMED.
C
      IMPLICIT COMPLEX*16 (C)
        IMPLICIT REAL*8(A-B,E-H,P-Z)
      DIMENSION XV1(NM),YV1(NM),XV2(NM),YV2(NM),Z(N,N)
      COMMON/NNN/NDP(10),BCOND(10,3),NTOTAL
        COMMON/TYPE/LAPOIS,EPSR
      C1=DCMPLX(1.D0,0.D0)
      CK=DCMPLX(100.D0,0.D0)
      PI=4.D0*DATAN(1.D0)
        NF=0
        DO 1000 JKLM=1,NTOTAL
        ALPHA=BCOND(JKLM,1)
        BETA=BCOND(JKLM,2)
        NI=NF+1
        NF=NF+NDP(JKLM)
      DO 999 I=NI,NF
C
C COMPUTE THE PARAMETERS OF THE FIELD SUBSECTION
C
        XI=XV1(I)
        XIP1=XV2(I)
        YI=YV1(I)
        YIP1=YV2(I)
        CZI=CMPLX(XI,YI)
        CZIP1=DCMPLX(XIP1,YIP1)
```

```
        EDELI=CDABS(CZIP1-CZI)
        CUI=(CZIP1-CZI)/EDELI
        CZICAR=(CZI+CZIP1)/2.D0
        DO 888 J=1,N
C
C COMPUTE THE PARAMETERS OF THE SOURCE SUBSECTION
C
        XJ=XV1(J)
        XJP1=XV2(J)
        YJ=YV1(J)
        YJP1=YV2(J)
        CZJ=DCMPLX(XJ,YJ)
        CZJP1=DCMPLX(XJP1,YJP1)
        EDELJ=CDABS(CZJP1-CZJ)
        CUJ=(CZJP1-CZJ)/EDELJ
        CARG=(CZICAR-CZJP1)/(CZICAR-CZJ)
C
        CTERM=CDLOG(CARG)/CUJ
        IF(BETA.EQ.0.D0)GO TO 666
        IF(I.EQ.J)EDERV=PI
        IF(I.NE.J)EDERV=DIMAG(CUI*CTERM)
        Z(I,J)=BETA*EDERV
        IF(ALPHA.EQ.0.D0)GO TO 888
CCCCCCCCCCCCC
666     CT1=(CZICAR-CZJ)*CTERM
        CT2=EDELJ*(1.D0+CDLOG(CK/(CZICAR-CZJP1)))
        Z(I,J)=Z(I,J)+ALPHA*DREAL(CT1+CT2)
C       IF(LAPOIS.EQ.1.AND.BETA.EQ.0.D0)Z(I,J)=10.0*Z(I,J)
888     CONTINUE
999     CONTINUE
1000    CONTINUE
        RETURN
        END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
        SUBROUTINE FIELD(RI,N,XV1,XV2,YV1,YV2,NM)
        IMPLICIT COMPLEX*16 (C)
        IMPLICIT REAL*8(A-B,E-H,P-Z)
        DIMENSION RI(N),XV1(NM),XV2(NM),YV1(NM),YV2(NM)
        COMMON/TYPE/LAPOIS,EPSR
        TPI=8.D0*DATAN(1.D0)
        IF(LAPOIS.EQ.1)TPI=TPI*EPSR*8.854D-12
        C1=(1.D0,0.D0)
        CK=(100.D0,0.D0)
C
C READ K=NO. OF POINTS AT WHICH FIELD AND POTENTIAL IS TO BE COMPUTED
C
        READ(92,*)XIN,YIN,XFIN,YFIN, K
        IF(K.EQ.1)IJKL=1
        IF(K.EQ.1)GO TO 78
        XDEL=(XFIN-XIN)/FLOAT(K-1)
        YDEL=(YFIN-YIN)/FLOAT(K-1)
78      CONTINUE
        DO 50 J=1,K
        X=(XIN+FLOAT(J-1)*XDEL)*1.D-06
        Y=(YIN+FLOAT(J-1)*YDEL)*1.D-06
        IF(K.EQ.1.AND.J.NE.1)GO TO 50
        CZK=DCMPLX(X,Y)
        SUMP=0.D0
        SUMX=0.D0
        SUMY=0.D0
```

```
      CZI=DCMPLX(XV1(I),YV1(I))
      CZIP1=DCMPLX(XV2(I),YV2(I))
      EDELI=CDABS(CZIP1-CZI)
      CUI=(CZIP1-CZI)/EDELI
      CARG=(CZK-CZIP1)/(CZK-CZI)
      CTERM0=CDLOG(CARG)/CUI
      CTERM=(CZK-CZI)*CTERM0
      CTERM2=EDELI*(C1+CDLOG(CK/(CZK-CZIP1)))
      CWI=CTERM+CTERM2
      SUMP=SUMP+RI(I)*DREAL(CWI)
      SUMX=SUMX+RI(I)*DREAL(CTERM0)
      SUMY=SUMY-RI(I)*DIMAG(CTERM0)
      SUMF=SQRT(SUMX*SUMX+SUMY*SUMY)
 45   CONTINUE
      SUMP=SUMP/TPI
      SUMX=SUMX/TPI
      SUMY=SUMY/TPI
      SUMF=SUMF/TPI
C     WRITE(18,55)CZK,SUMP,SUMX,SUMY,SUMF
      IF(LAPOIS.EQ.0)GO TO 50
      CALL POTEN(X,Y,SP)
      SUMP=SUMP+SP/TPI
      WRITE(18,49)X,Y,SUMP
 49   FORMAT(3X,'X=',E11.5,2X,'Y=',E11.5,3X,'TOTAL POT=',E11.4,/)
 50   CONTINUE
 55   FORMAT(1X,'Z=',2E11.5,3X,'POT=',E10.4,3X,'EX=',E10.4,2X,
     6 'EY=',E10.4,3X,'ETOT=',E10.4)
      RETURN
      END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      SUBROUTINE ELSV(A,B,C,N,DE,EP)
      IMPLICIT REAL*8(A-H,P-Z)
      DIMENSION A(N,N),B(N),C(N)
      DO 11 I=1,N
      B(I)=0.D0
      C(I)=0.D0
      DO 12 J=1,N
 12   C(I)=C(I)+A(I,J)
 11   A(I,I)=A(I,I)-1.D0
      DO 13 K=1,N
      DO 14 J=1,N
      B(J)=A(K,J)
 14   A(K,J)=0.D0
      A(K,K)=1.D0
      W=B(K)+1.D0
      IF(ABS(W).LT.EP)GO TO 17
      DO 13 I=1,N
      Y=A(I,K)/W
      DO 13 J=1,N
 13   A(I,J)=A(I,J)-B(J)*Y
      DE=0.D0
      DO 15 J=1,N
      B(J)=0.D0
      DO 16 I=1,N
 16   B(J)=B(J)+A(I,J)
 15   DE=DE+C(J)*B(J)
      RETURN
 17   DE=-1.D0
      RETURN
```

```
      IMPLICIT COMPLEX*16 (C)
      IMPLICIT REAL*8 (A-B,E-H,P-Z)
C
C
C THIS PROGRAM GIVES THE POTENTIAL AND THE
C GRADIENT OF THE POTENTIAL PRODUCED BY A
C CERTAIN TWO DIMENSIONAL CHARGE DISTRIBUTION
C AT A POINT (X,Y).
C
C NOTE THAT AS THE CHARGE DISTRIBUTION IS CHANGED
C THIS PROGRAM SHOULD BE CHANGED ACCORDINGLY.
C
C THIS PROGRAM WILL BE CALLED BY THE PROGRAM NAMED
C 'DNEWPOISSON' ONLY IF THE PARAMETER LAPOIS IS 1 IN
C THAT PROGRAM.
C
      RHO=-3200.D0
      AK=100.D0
      X1=-0.50D-06
      Y1=-0.04D-06
      X2=0.5D-06
      Y2=0.04D-06
CCCCCCCCCCCCCCCCCCC
      POT=(Y2-Y1)*(X2-X1)*DLOG(AK)
CCCCCCCCCCCCCCCCCCC
      EDEL1=DABS(X2-X1)
      U1=(X2-X1)/EDEL1
CCCCCCCCCCCCCCCCCCC
      FI1=(Y2-Y1)
      POT=POT+EDEL1*FI1
CCCCCCCCCCCCCCCCCCC
      CZ3=DCMPLX(X2,Y1)
      CZ4=DCMPLX(X2,Y2)
      CZ=DCMPLX(X,Y)
      EDEL2=CDABS(CZ4-CZ3)
      CU2=(CZ4-CZ3)/EDEL2
      CT2=(CZ-CZ3)*CDLOG((CZ-CZ4)/(CZ-CZ3))/CU2
      CT2=CT2+EDEL2*(1.D0-CDLOG(CZ-CZ4))
CCCCCCCCCCCCCCCCCCCCC
      FI2=DREAL(CT2)
      FI31=(X1-X)*FI2
      POT=POT+EDEL1*FI2+FI31/U1
CCCCCCCCCCCCCCCCCCCCC
      XS=X2
      CALL INTG(XS,Y1,Y2,X,Y,RES32)
CCCCCCCCCCCCCCCCCCCCCC
      FI32=RES32
      POT=POT+FI32/U1
CCCCCCCCCCCCCCCCCCCCC
      CZ5=DCMPLX(X1,Y1)
      CZ6=DCMPLX(X1,Y2)
      EDEL3=CDABS(CZ6-CZ5)
      CU3=(CZ6-CZ5)/EDEL3
      CT41=(CZ-CZ5)*CDLOG((CZ-CZ6)/(CZ-CZ5))/CU3
      CT41=CT41+EDEL3*(1.D0-CDLOG(CZ-CZ6))
CCCCCCCCCCCCCCCCCCCCCC
      FI41=(X1-X)*DREAL(CT41)
      POT=POT-FI41/U1
CCCCCCCCCCCCCCCCCCCCCC
```

```
      CALL INTG(XS,Y1,Y2,X,Y,RES42)
CCCCCCCCCCCCCCCCCCCCCCCCCCCC
      FI42=RES42
      POT=POT-FI42/U1
      POT=RHO*POT
      RETURN
      END
      SUBROUTINE INTG(XS,Y1,Y2,X,Y,RES)
      IMPLICIT REAL*8(A-B,E-H,P-Z)
      PI=4.D0*DATAN(1.D0)
      TP=2.D0*PI
      PO2=PI/2.D0
      PO4=PI/4.D0
      IF(X-XS)20,10,15
 10   IF(Y.GE.Y2)RES=PO4*((Y2-Y)*(Y2-Y)-(Y1-Y)*(Y1-Y))
      IF(Y.LE.Y1)RES=-PO4*((Y2-Y)*(Y2-Y)-(Y1-Y)*(Y1-Y))
      IF(Y.GT.Y1.AND.Y.LT.Y2)IM=1
      IF(IM.EQ.1)RES=-PO4*((Y2-Y)*(Y2-Y)+(Y1-Y)*(Y1-Y))
      RETURN
 15   T1=(X-XS)*(Y2-Y1)
      T2=(Y-Y2)*(Y-Y2)+(X-XS)*(X-XS)
      T3=(Y-Y1)*(Y-Y1)+(X-XS)*(X-XS)
      T4=(Y2-Y)/(X-XS)
      T5=(Y1-Y)/(X-XS)
      IF(Y.GE.Y2)RES=(T1-T2*DATAN(T4)+T3*DATAN(T5))/2.D0
      IF(Y.LE.Y1)RES=(T1-T2*DATAN(T4)+T3*DATAN(T5))/2.D0
      IF(Y.GT.Y1.AND.Y.LT.Y2)IM=1
      IF(IM.EQ.1)RES=(T1+T3*DATAN(T5)-T2*DATAN(T4))/2.D0
      RETURN
 20   T1=(XS-X)*(Y2-Y1)
      T2=(Y2-Y)*(Y2-Y)+(XS-X)*(XS-X)
      T3=(Y-Y1)*(Y-Y1)+(XS-X)*(XS-X)
      T4=(Y2-Y)/(XS-X)
      T5=(Y1-Y)/(XS-X)
      TERM=PO2*((Y2-Y)*(Y2-Y)-(Y1-Y)*(Y1-Y))
      IF(Y.GE.Y2)RES=TERM-(T1-T2*DATAN(T4)+T3*DATAN(T5))/2.D0
      IF(Y.LE.Y1)RES=-TERM+(T2*DATAN(T4)-T1-T3*DATAN(T5))/2.D0
      IF(Y.LT.Y2.AND.Y.GT.Y1)IM=1
      IF(IM.EQ.1)TM=-PO2*((Y1-Y)*(Y1-Y)+(Y2-Y)*(Y2-Y))
      IF(IM.EQ.1)RES=TM-(T1+T3*DATAN(T5)-T2*DATAN(T4))/2.D0
      RETURN
      END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      SUBROUTINE GRAD(X,Y,GX,GY)
      implicit complex*16 (c)
      IMPLICIT REAL*8(A-B,E-H,P-Z)
      RHO=-3200.D0
      C2=DCMPLX(X,Y)
      X1=-0.50D-06
      Y1=-0.04D-06
      X2=0.5D-06
      Y2=0.04D-06
      CZ1=DCMPLX(X1,Y1)
      CZ2=DCMPLX(X2,Y1)
      CZ3=DCMPLX(X1,Y2)
      CZ4=DCMPLX(X2,Y2)
      EDEL1=CDABS(CZ2-CZ1)
      CU1=(CZ2-CZ1)/EDEL1
      EDEL2=CDABS(CZ4-CZ3)
```

```
      CU2=(CZ4-CZ3)/EDEL2
      CTERM1=(CZ-CZ1)*CDLOG((CZ-CZ2)/(CZ-CZ1))/CU1
      CTERM1=CTERM1+EDEL1*(1.D0+CDLOG(1.D0/(CZ-CZ2)))
      CTERM2=(CZ-CZ3)*CDLOG((CZ-CZ4)/(CZ-CZ3))/CU2
      CTERM2=CTERM2+EDEL2*(1.D0+CDLOG(1.D0/(CZ-CZ4)))
      GY=-RHO*DREAL(CTERM2-CTERM1)
      GX=0.D0
      RETURN
      END
```

SAMPLE INPUT/OUTPUT FILE:

The following is the input/output file for the long channel MOSFET problem considered in Fig. 4. The results presented in the following are plotted in Fig. 6 and 7.

```
4  11.750 1
0.5 -0.106  0.5 0.106  12
1.0 0.0 5.9
-0.5 0.106 -0.5 -0.106 12
1.0 0.0 0.9
-0.5 -0.106 0.5 -0.106 25
0.0 1.0 0.0
0.5  0.106  -0.5  0.106  25
1.0 0.22E-06  2.0
-0.50 0.1059999 0.50 0.105999 21
```

```
 X=-.50000E-06  Y=0.10600E-06   TOTAL POT= 0.9552E+00
 X=-.45000E-06  Y=0.10600E-06   TOTAL POT= 0.1016E+01
 X=-.40000E-06  Y=0.10600E-06   TOTAL POT= 0.1005E+01
 X=-.35000E-06  Y=0.10600E-06   TOTAL POT= 0.9841E+00
 X=-.30000E-06  Y=0.10600E-06   TOTAL POT= 0.9704E+00
 X=-.25000E-06  Y=0.10600E-06   TOTAL POT= 0.9691E+00
 X=-.20000E-06  Y=0.10600E-06   TOTAL POT= 0.9827E+00
 X=-.15000E-06  Y=0.10600E-06   TOTAL POT= 0.1012E+01
 X=-.10000E-06  Y=0.10600E-06   TOTAL POT= 0.1059E+01
 X=-.50000E-07  Y=0.10600E-06   TOTAL POT= 0.1126E+01
 X=0.00000E+00  Y=0.10600E-06   TOTAL POT= 0.1216E+01
 X=0.50000E-07  Y=0.10600E-06   TOTAL POT= 0.1332E+01
 X=0.10000E-06  Y=0.10600E-06   TOTAL POT= 0.1478E+01
 X=0.15000E-06  Y=0.10600E-06   TOTAL POT= 0.1661E+01
 X=0.20000E-06  Y=0.10600E-06   TOTAL POT= 0.1891E+01
 X=0.25000E-06  Y=0.10600E-06   TOTAL POT= 0.2178E+01
 X=0.30000E-06  Y=0.10600E-06   TOTAL POT= 0.2534E+01
 X=0.35000E-06  Y=0.10600E-06   TOTAL POT= 0.2986E+01
 X=0.40000E-06  Y=0.10600E-06   TOTAL POT= 0.3575E+01
 X=0.45000E-06  Y=0.10600E-06   TOTAL POT= 0.4387E+01
 X=0.50000E-06  Y=0.10600E-06   TOTAL POT= 0.5556E+01
```

```
2.5 -0.106  2.5 0.106  12
1.0 0.0 5.9
-2.5 0.106 -2.5 -0.106 12
1.0 0.0 0.9
-2.5 -0.106 2.5 -0.106 50
0.0 1.0 0.0
  5  0.106  -2.5  0.106  50
1.0 0.22E-06  2.0
-2.50 0.1059999 2.50 0.105999 21
```

```
 X=-.25000E-05  Y=0.10600E-06   TOTAL POT= 0.9238E+00
 X=-.22500E-05  Y=0.10600E-06   TOTAL POT= 0.7867E+00
 X=-.20000E-05  Y=0.10600E-06   TOTAL POT= 0.6475E+00
 X=-.17500E-05  Y=0.10600E-06   TOTAL POT= 0.5955E+00
 X=-.15000E-05  Y=0.10600E-06   TOTAL POT= 0.5764E+00
 X=-.12500E-05  Y=0.10600E-06   TOTAL POT= 0.5694E+00
 X=-.10000E-05  Y=0.10600E-06   TOTAL POT= 0.5669E+00
 X=-.75000E-06  Y=0.10600E-06   TOTAL POT= 0.5659E+00
 X=-.50000E-06  Y=0.10600E-06   TOTAL POT= 0.5656E+00
 X=-.25000E-06  Y=0.10600E-06   TOTAL POT= 0.5655E+00
 X=0.00000E+00  Y=0.10600E-06   TOTAL POT= 0.5656E+00
 X=0.25000E-06  Y=0.10600E-06   TOTAL POT= 0.5659E+00
 X=0.50000E-06  Y=0.10600E-06   TOTAL POT= 0.5667E+00
 X=0.75000E-06  Y=0.10600E-06   TOTAL POT= 0.5692E+00
 X=0.10000E-05  Y=0.10600E-06   TOTAL POT= 0.5758E+00
 X=0.12500E-05  Y=0.10600E-06   TOTAL POT= 0.5940E+00
 X=0.15000E-05  Y=0.10600E-06   TOTAL POT= 0.6434E+00
 X=0.17500E-05  Y=0.10600E-06   TOTAL POT= 0.7788E+00
 X=0.20000E-05  Y=0.10600E-06   TOTAL POT= 0.1147E+01
 X=0.22500E-05  Y=0.10600E-06   TOTAL POT= 0.2158E+01
 X=0.25000E-05  Y=0.10600E-06   TOTAL POT= 0.5499E+01
```

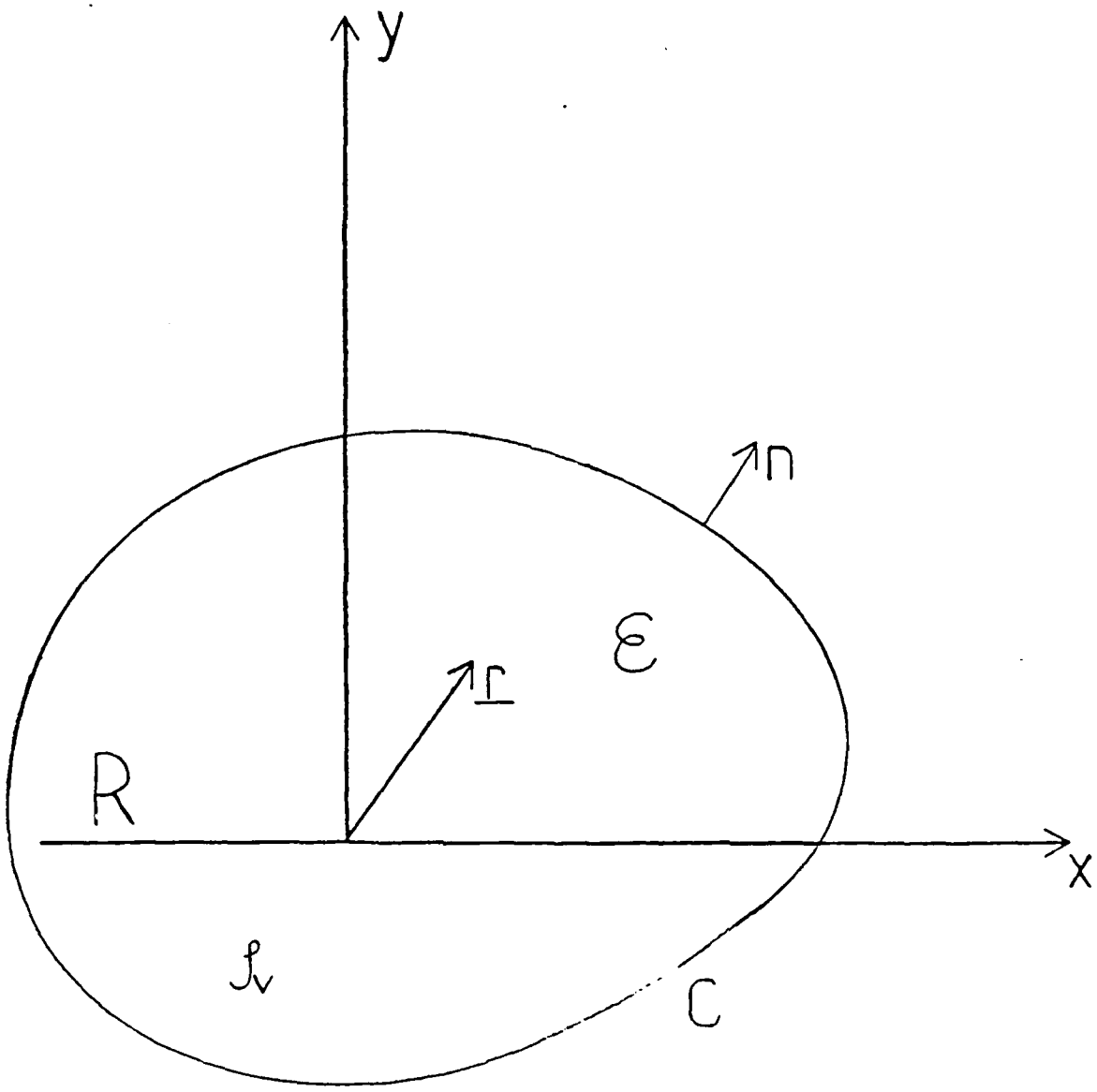


Fig. 1. Geometry of the problem.

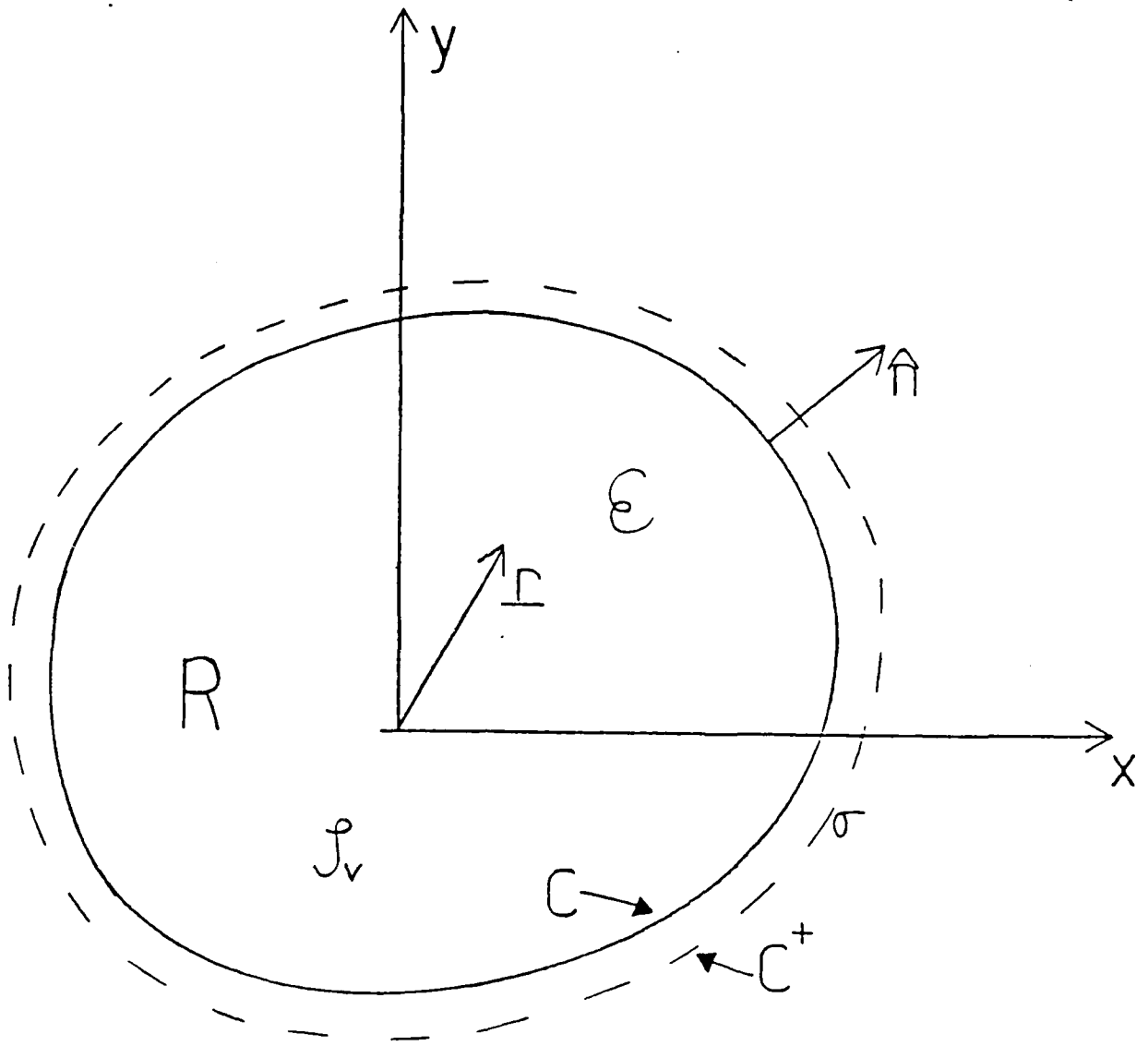


Fig. 2. The potential in R is produced by the impressed volume charges ρ_v and the equivalent surface charges σ. The surface charges are on C^+, (just outside of bounding surface C).

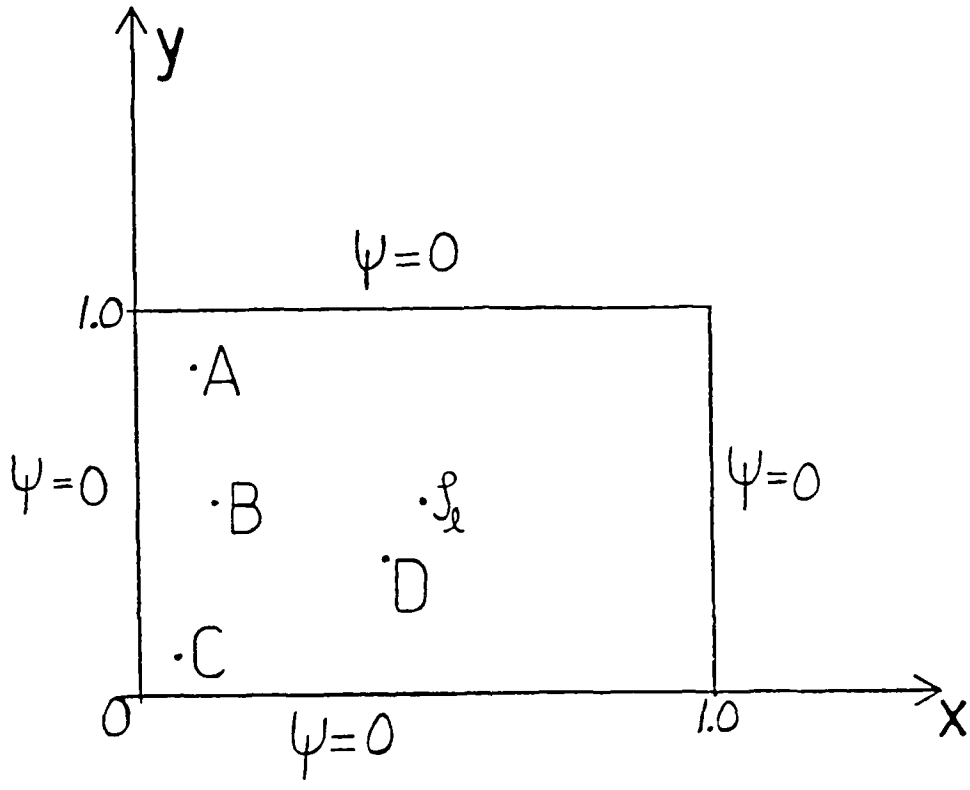


Fig. 3. A line charge at the center of an infinitely long grounded, rectangular pipe.

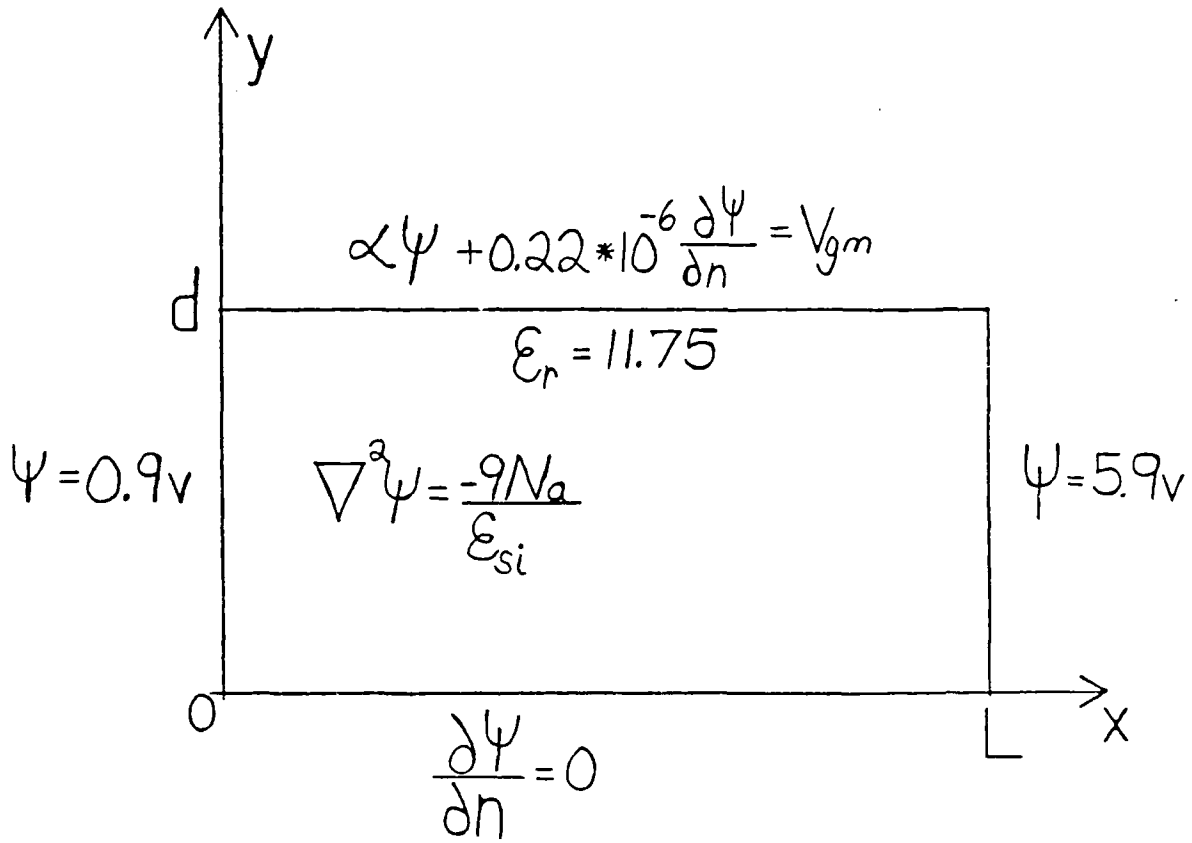


Fig. 4. An approximate model for a rectangular depletion region in a MOSFET.

($E_{si} = E_o E_r$, $9\ Na = -3200.0\ C/3_m$)

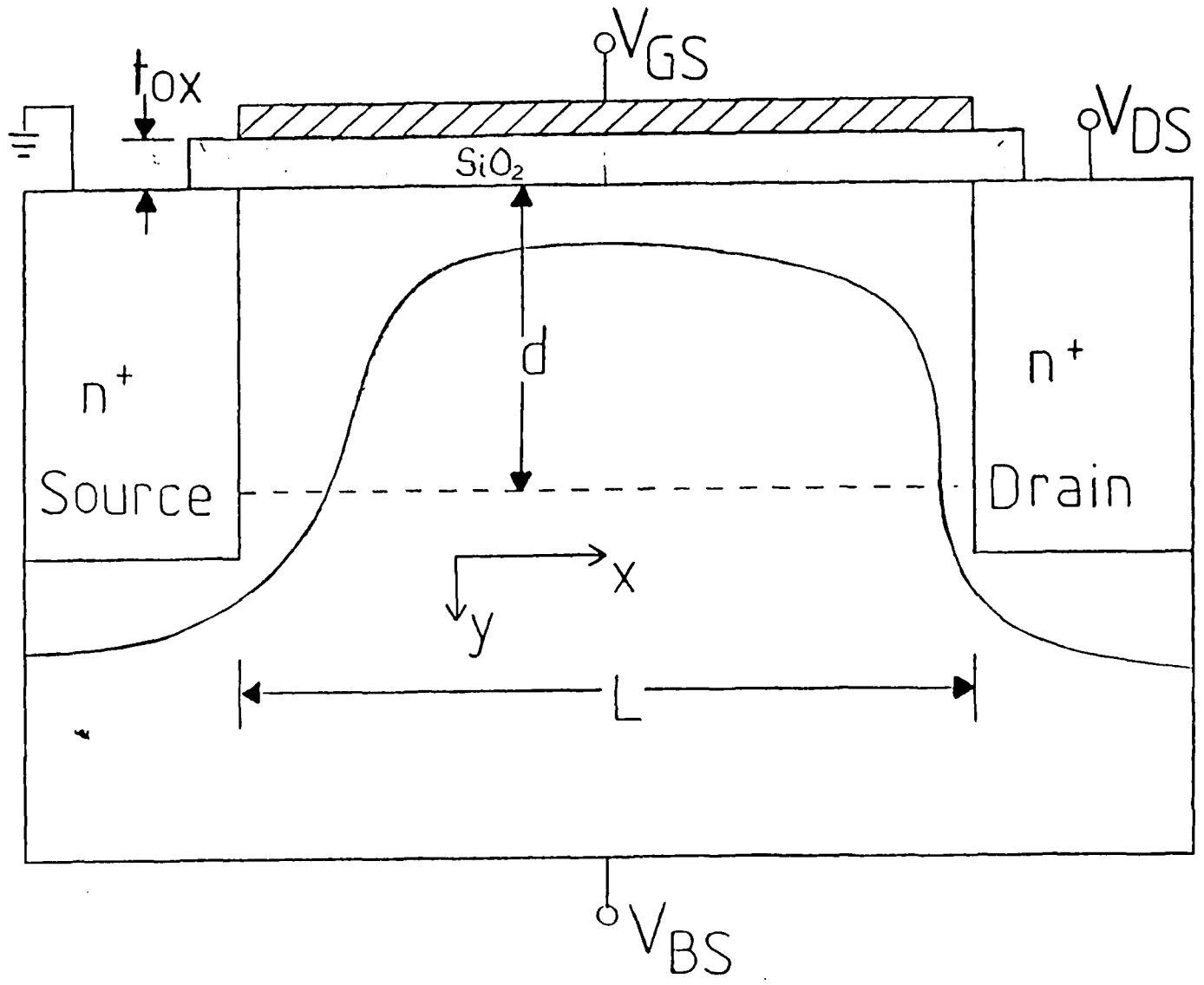


Fig. 5. Rectangular Depletion Region under the gate of an N-Channel MOSFET

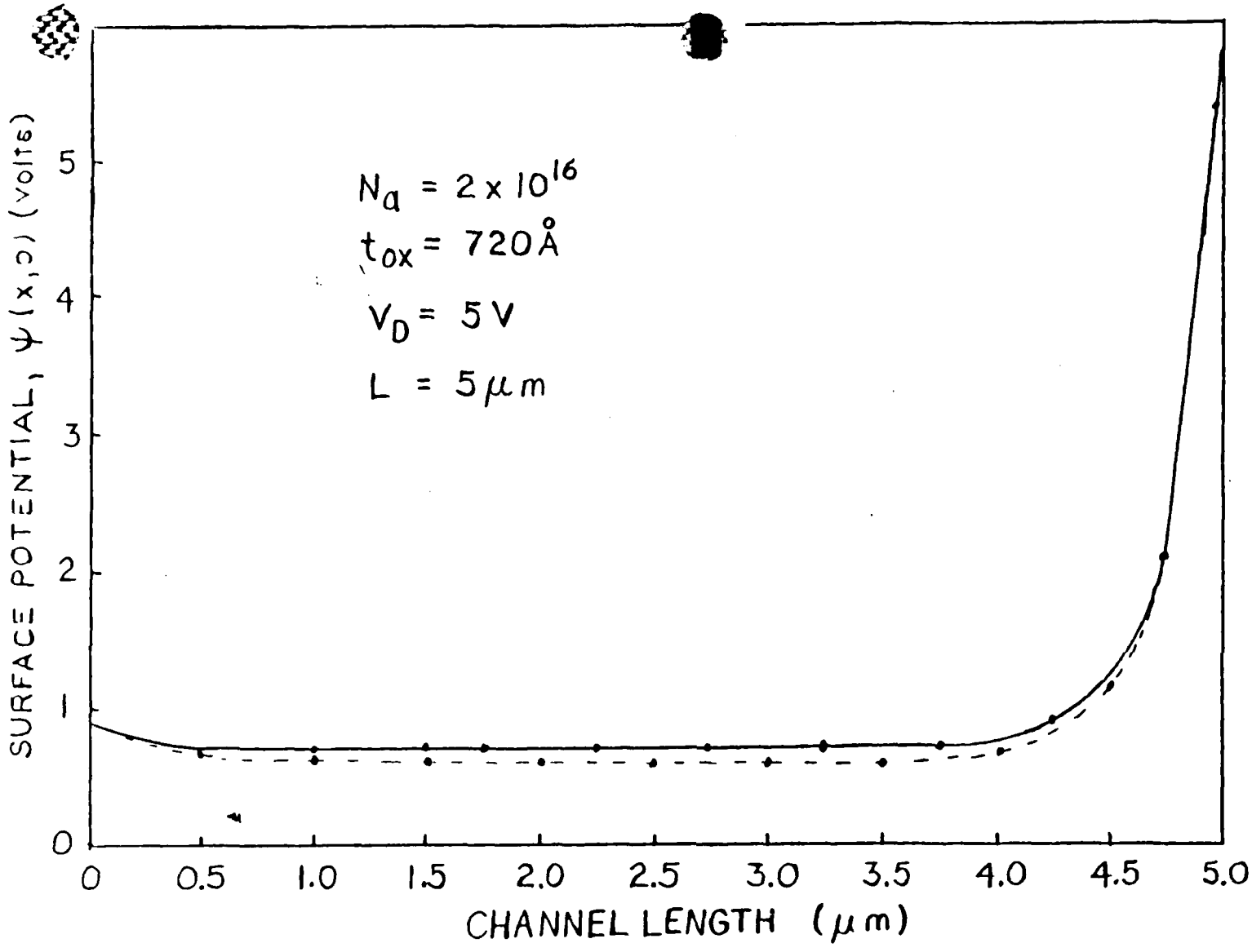


Fig. 6. Surface Potential Variation Along the Channel for a 1 μ m Device

_____ Poole & Kwang (Ref. 4)
●...●...● Present Method

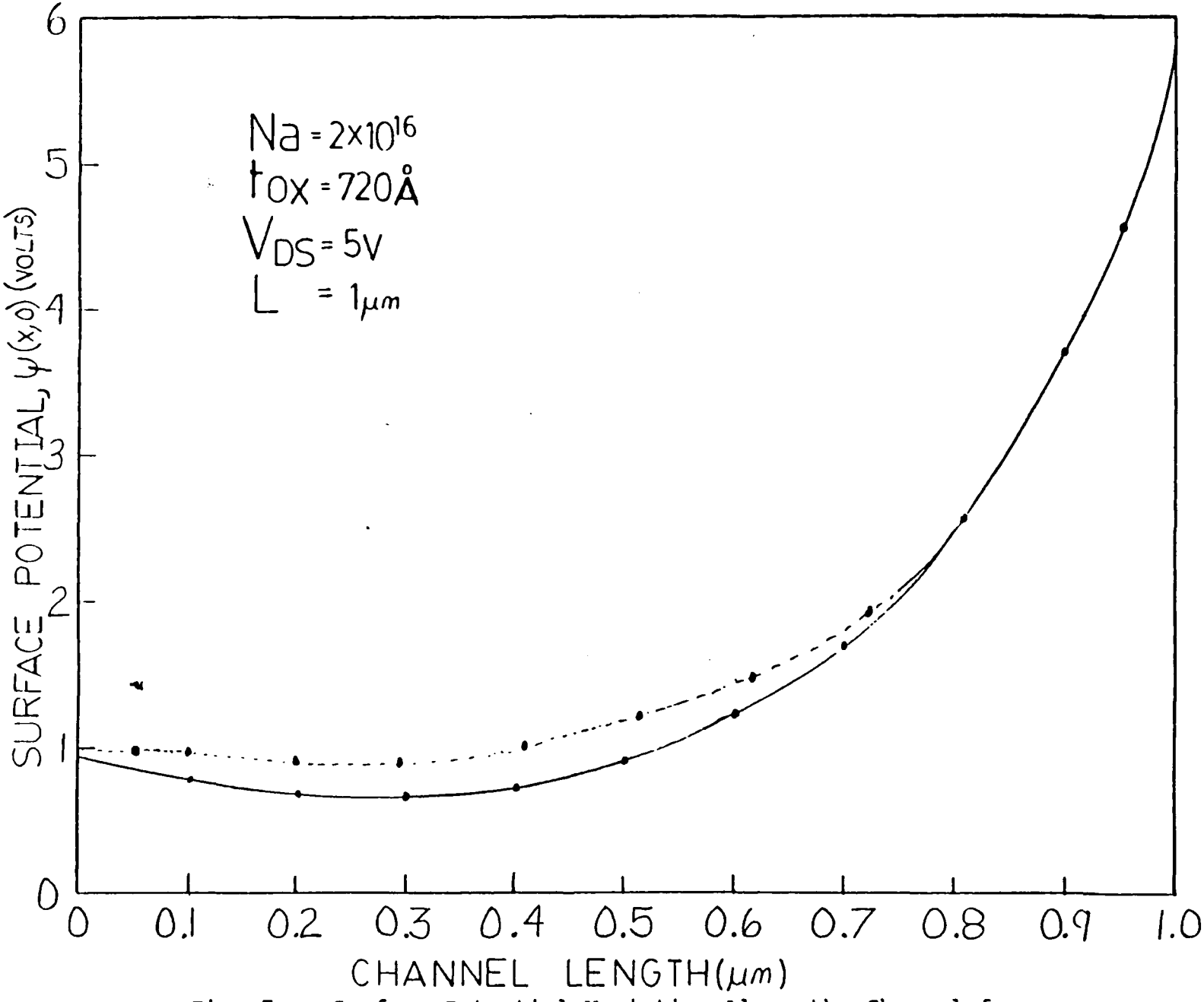


Fig. 7. Surface Potential Variation Along the Channel for a 5 μ m Device

Poole & Kwang (Ref. 4)

Present Method

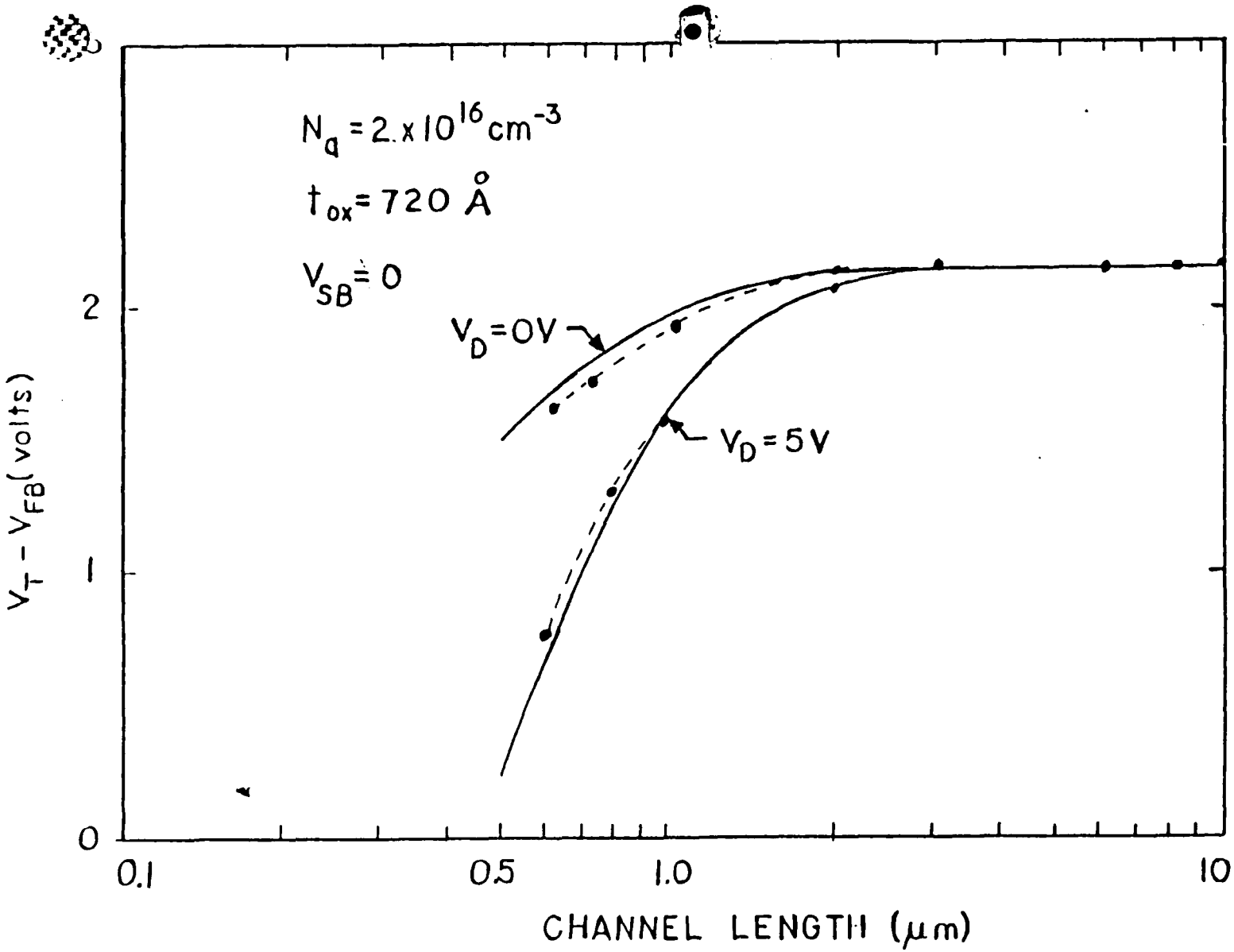


Fig. 8. Threshold Voltage Versus Channel Length for Drain Voltage (V_D) of 0 & 5V

———— Poole & Kwang (Ref. 4)

●...●...● Present Method

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Susceptibility of a class of bipolar RF power transistors (known as stripline-opposed emitter (SOE) devices) to electrical overstressing (EOS) is studied. By virtue of having unique packaging compatible for RF/stripline applications, SOE devices pose prominent/extended exteriors for static propensity and hence are critically vulnerable to damages/degradation as predictable by the

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charged-device modeling. As such, contrary to the popular notion that rugged bipolar devices are not excessively prone to ESD-based detrimental effects, SOE transistors, on the other hand, are severely vulnerable to EOS threats. It is not just the Wunsch-Bell limit of catastrophy due to PN junction burnout (under high-level zaps) that dictates the damages in the devices like SOE transistors. The entire device configuration, namely, active junction, metallization, bonding, etc., as well as the external packaging, decide the device lethality. This is demonstrated by experimental studies on a family of SOE devices by subjecting them to ESD zaps using a Human Body Simulator. The results positively indicate that their vulnerability is in excess of Class II limit specified by DOD-HDBK-263 and require specific handling precautions, lest they would pose quality control and/or field failure problems. Especially, considering these devices being extremely costly, specific ESD control efforts are rather imminent.

ESD/EOS SUSCEPTIBILITY OF A CLASS OF BIPOLAR RF POWER TRANSISTORS: EXPERIMENTAL STUDIES ON STRIPLINE-OPPOSED EMITTER TRANSISTORS

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ABSTRACT

Susceptibility of a class of bipolar RF power transistors (known as stripline-opposed emitter (SOE) devices) to electrical overstressing (EOS) is studied. By virtue of having unique packaging compatible for RF/stripline applications, SOE devices pose prominent/extended exteriors for static propensity and hence are critically vulnerable to damages/degradation as predictable by the charged-device modeling. As such, contrary to the popular notion that rugged bipolar devices are not excessively prone to ESD-based detrimental effects, SOE transistors, on the other hand, are severely vulnerable to EOS threats. It is not just the Wunsch-Bell limit of

catastrophy due to PN junction burnout (under high-level zaps) that dicates the damages in the devices like SOE transistors. The entire device configuration, namely, active junction, metallization, bonding, etc., as well as the external packaging, decide the device lethality. This is demonstrated by experimental studies on a family of SOE devices by subjecting them to ESD zaps using a Human Body Simulator. The results positively indicate that their vulnerability is in excess of Class II limit specified by DOD-HDBK-263 and require specific handling precautions, lest they would pose quality control and/or field failure problems. Especially, considering these devices being extremely costly, specific ESD control efforts are rather imminent.

INTRODUCTION

This work addresses the proneness to ESD/EOS of certain bipolar devices used in RF power amplification, commonly known as stripline-opposed emitter (SOE) transistors. These devices have characteristic packagings as depicted in Fig. 1. They are silicon transistors designed for high efficiency, high linearity Class A-power amplification at UHF bands [1].

The primary electrical advantage of the SOE packages are the low inductance stripline leads which interface very well with the microstriplines often used in UHF/VHF equipment and the good collector to base isolation provided by the two emitter leads. The two-emitter concept promotes symmetry in board layout when combining devices to obtain higher

power output. Further, stud and/or flange-mounting feasibility of SOE devices permit excellent heat-sinking and hence high thermal performance.

While the aforesaid characteristics allow popular use of the SOE devices for the purpose of RF power amplification, there is no available data regarding their performance under electrostatic discharge (ESD)/electrical overstressing (EOS) environment. Like any bipolar device, per DOD-HDBK-263, these devices may, in general, fall under Class II category [2] of components in respect of their ESD/EOS proneness. However, this generalization needs to be verified because the peculiar package-geometry pose a prominent/extended cross-section of exposure to the static environment. As such, the severity of ESD damage in such bipolar devices would be reduced not only by the Wunsch-Bell limits of catastrophy [3] at the PN junction [4], but also by the static propensity and parasitic (shunt) paths of static-discharge associated with the device package. Further, the inherent capacitive and/or inductive reactance of the device-exterior will profusely influence the static discharge characteristics and hence the relevant ESD-based stressings on the device.

Thus the present work will decide whether SOE packaged bipolar devices be classified under general Class II type of ESD-prone components as listed in the DOD-HDBK-263. Relevant effort will also explicitly determine the effect of performance-based packaging on the device vulnerability to ESD/EOS.

In SOE devices, the junctions are designed enough to carry a sustained current flow of about 1 ampere, compatible for high power applications. Therefore, the possibility of total junction burnout (Wunsch-Bell limit) by ESD zaps may not be anticipated. However, considering the total device geometry (with its constricted regions, bond/metallization regions, etc.), vulnerability of the device to ESD-based damages cannot be ruled out, especially due to the presence of high static propensive exterior (packaging). Hence, the present investigations are done on the devices subjecting them to simulated ESD zaps to evaluate their proneness to EOS damages.

EXPERIMENTAL STUDIES

The test transistors considered are: ENI 10A, ENI 14B and ENI 2240. These devices form a class of bipolar active elements intended for applications with high performance thermal and high frequency characteristics. They have typical stripline opposed emitter (SOE) packaging designed for interfacing with microstriplines and for good thermal dissipative capabilities.

Prezap Tests:

The static characteristics, as well as the transistor gain h_{FE}, were measured prior to the application of zaps. The unstressed device

characteristics indicate that for a given type of transistor, the reverse-bias leakage current varies widely from piece-to-piece at ambient conditions. The reverse breakdown also ranged from abrupt to smooth artifacts. In some cases, ohmic short across base-emitter (B-E) junctions were observed.

The prezap test results are presented in Tables 1 to 3 and the prezap test is labelled as 'a' in the test sequence.

Zap Tests:

The zap tests were performed on the devices using an ESD human-body simulator (Model: IMCS2400). This equipment simulates the transient discharge characteristics which is a close representation of the ESD event pertaining to the static discharge from a human body. The simulator circuit (per MIL-M-38150) [2] is depicted in Fig. 2.

Testing methods are documented [2] in DOD-HDBK-263, Art. 6.2. Normally ESD-based part failure is defined as the inability of a part to meet the electrical parameter limits of the part specifications. Any measurable change in a part electrical parameter due to an ESD could like an indication of part damage and susceptibility to further degradation and subsequent failure with successive ESD.

Hence using the standard ESD Simulator (Model: IMCS2400), the test devices were subjected to various combinations (in terms of polarity, amplitude, multiplicity, etc.) of ESD zaps. (Prior to overstressing, the devices were assessed for their characteristics, as mentioned earlier under 'Prezap Tests').

The characteristics of the devices after each mode of test were measured using the Semiconductor Parameter Analyzer Model: HP4145. These results are presented in Tables 1-3. The sequence of tests conducted after overstressing are referred to as b, c, d, e, f, and g.

Tables 1-3 provide the complete compilation of test data and summarize the results. The recorded characteristics are depicted in a few sets of figures appended. Each set of figures is identified by the device type/number, the sample number, and the test sequence. For example, Fig. A 1.b denotes the characteristics of the transistor A (ENI 10A), sample number 1, after the overstressing sequence of 'b,' as described in Table 1. Likewise, B refers to transistor ENI 14B, and C denotes ENI 2240.

OBSERVATIONS

a. The tested devices are prone to ESD-based failures and/or degradations.

b. Low level zaps cause no catastrophic damages. However, the devices are susceptible for catastrophic failures at high zap levels which can be anticipated at low humidity situations.

c. The degradation is cumulative but stabilizes after a few multiple zaps. Up to 20% change in h_{FE} and a more serious variation of I_{EBO} (leakage current) changing in excess of 100% were observed.

d. Polarity Dependence: Zaps of alternating polarities appear to influence the degradation to a larger extent. (The probabilities of occurrence of positive and negative zaps can be anticipated to be the same in practice.)

e. Multiple single polarity zaps of larger magnitude do not cause more harm than low intensity, multiple zaps of bidirectional polarity.

f. Isolated single zaps appear to cause no damage (even on already wounded devices).

g. Frequent manual handling of the devices with the possibilities of applying zaps of bidirectional polarities in a sequence, would damage them to a maximum extent.

h. The devices are more prone to damages while receiving a set of initial zaps. Subsequent zaps may not influence any further degradation. However, the devices pose high probabilities of receiving initial zaps anywhere in the production/manufacturing, shipping or assembly lines.

i. The devices can be subjected to harmful zaps at subassembly/PCB levels. However, their chances of getting degraded by single or multiple zaps at equipment level are rather remote.

j. Devices which exhibit base-emitter ohmic leakage during prezap screen, have been observed to suffer higher damages, even at low or subcatastrophic ESD levels.

k. Description of observed damages in these test devices:

Noncatastrophic ESD-Human Body model zaps applied between the base the the emitter of the transistors with serial numbers ENI 10A and ENI 14B caused these devices to exhibit lower h_{FE} and/or larger base-emitter junction leakage current. ESD pulses that forward biased the B-E junction, lowered the h_{FE} without significantly increasing the leakage current while pulses of reverse biasing polarity degraded the B-E junction's characteristics invariably without affecting the transistor gain at nominal current levels.

ESD pulses of reverse polarity did also affect the low current level transistor gain. The observation can be explained as follows:

1. When a reverse biasing ESD pulse is applied to the junction, most of the power dissipation occurs within the depletion layer where the electric field intensity is maximum. The temperature rise and the subsequent crystal damage in the form of increased recombination/generation centers can be anticipated to be very high in the vicinity of the junction. Therefore, junction leakage current which is predominately controlled by carriers that are generated within the depletion region increases.

2. The transistor gain at nominal current levels does not depend on depletion layer parameters and therefore, it is not sensitive to reverse biasing ESD pulses.

3. The reason for transistor gain being lower at low current densities is the significant loss of injected carriers by recombination across the B-E junction's depletion layer; this parameter drops when reverse biasing ESD pulses are applied to the junction.

4. The test transistors are made by planar technology. The curved edges of the junctions are the most vulnerable regions in reverse bias; the reverse breakdown occurs first at these edges and most of the ESD transient current flows through edge regions.

   The rest of the junction, as well as the bulk of the emitter and the base, are however, much less affected. As the transistor gain at nominal current depends mainly on what occurs in these regions, this parameter is not very sensitive to ESD pulses of reverse polarity.

5. The transient current during forward biasing due to ESD zaps flows through the entire junction area and degrades the bulk of the emitter and the base, thus affecting h_{FE} at all current levels.

The catastrophic failures observed with the transistors ENI 10A and ENI 14B are due to the (emitter) contact metallization penetrating into silicon and introducing an ohmic low resistance path across the B-E junction. This metal-silicon alloy spike(s) penetrate deep into the base, even reaching the base-collector junction depletion layer, thus, severly affecting current-voltage characteristics at this junction.

Regarding the transistor ENI 2240, the observed latent failures were due to an increased wire/thin film and/or thin film metallization/silicon contact resistance. Both the emitter and the base contacts displayed this sort of vulnerability to ESD zaps. The contact fatigue increased gradually with repetitive ESD zaps, resulting in an undue increase in contact resistance values. As a result, larger V_{CE} values were needed to pull the transistor out of saturation (an increasingly larger portion of the applied V_{CE} dropped at the contacts, rather than appearing across the internal PN junctions). The excessive Joule heating at the contacts resulted in the penetration of the thin film metallization into the silicon. Low resistance paths were found across the B-E and/or B-C junction of the devices that suffered catastrophic failures.

DEVICE HANDLING: SUGGESTIONS

1. Inasmuch as the test devices indicated proneness to wounding and/or catastrophic failures under ESD zaps, proper handling procedure is suggested.

2. Though classified as Class II, the test devices being costly semiconductors be packaged, transported and handled with necessary care as specified in DOD-HDBK-263.

3. Part Screening: Some of the devices tested exhibit bypass leakage characteristics across B-E junction (e.g. ENI 10A) prior to zapping. This could have resulted from improper handling (?). Another test piece having normal prezap characteristics was zapped (ESD-HBM Test Voltage 16KV peak, multiple) and showed similar wounded ohmic characteristics. Therefore, it is suggested that for reliable circuit operation, devices which could have been damaged earlier either due to ESD or otherwise may be screened out via simple base-emitter I-V characteristic tests enabling the rejections of damaged pieces.

4. ENI 2240 shows contact and/or metallization based vulnerability to damages under EOS. Test results indicate contact and/or metallization resistance increasing cumulatively with number of zaps. Hence, it limits the $I_{c\ max}$ capability of the device to a significant extent and makes it unsuitable for large-signal applications. Both emitter and collector pose the above enhanced contact/metallization resistance problem. In this point of view, use of ENI 2240 may be carefully reviewed.

REFERENCES

[1] Motorola Semiconductors: Product Review on MRF Series

[2] DOD-HDBK-263: Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment.

[3] D.C. Wunsch and R.R. Bell: Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors due to Pulse Power Voltages, IEEE Trans. Nucl. Sci., NS-15(6), pp 244-259 (1968).

[4] W.J. Orvis, et al: A Review of the Physics and Response Models for Burnout of Semiconductor Devices, Final Report: UCRL-53573, Lawrence Livermore National Laboratory, UCLA, CA 94880, (December 1984).

DEVICE UNDER TEST: ENI 10A RF POWER TRANSISTOR # A

TABLE 1

Sample No	Measured Prezap Data [a]		ESD - Human Body Model Zap Tests & Results							Comments	Remarks
			Test Sequences								
	h_{Fe} @ 80 MA	I_{EBO}		b	c	d	e	f	g		
1	45	IμA	Parameters / Tests	5 zaps @ ± 50V to ± 16KV Assorted	25 zaps @ + 16KV	5 zaps @ -16KV	15 zaps @ 16KV	-	-	[b] Base-Emitter Short	1 For all the devices zaps are applied between Base & Emitter unless otherwise specified 2 Relevant to the test sequences indicated the measured graphical data are depicted in Figs. A.1.a to Figs. A.1.a to A.5.d
		@	h_{FE}	No Change	40	36	Catastro-	-	-		
		-5.6V	I_{EBO}	No Change	No Change	2.2μA	-phic Damage	-	-		
2	47	2.3μA	Parameters / Tests	5 zaps @ 50V to + 16KV Assorted	5 zaps @ -16KV	15 zaps @ -16KV	20 zaps @ +16KV	15 zaps at -16KV	5 zaps @ +10KV & -10KV alternate	[b] Base-Emitter Short (80 ohms)	
		@	h_{FE}	No Change	No Change	No Change	No Change	23 @ 50MA	catastrophic Damage		
		-5.6V	I_{EBO}	No Change	65μA	7.5μA	No Change	125μA			
3	44	100μA	Parameters / Tests	5 zaps + 10KV & -10KV Alternate	30 zaps @ ± 10KV	5 zaps @ -16KV	-	-	-	a] Prezap test indicates ohmic B-E leakage (23K Ω) b] Base-Emitter Short (80 ohms)	
		@	h_{FE}	No Change	No Change	Catastrophic Damage	-	-	-		
		-2.5V	I_{EBO}	450μA	No Change		-	-	-		
4	44	1.2 A	Parameters / Tests	5 zaps @ ± 7KV	10 zaps @ ± 7KV	70 zaps @ ± 7 KV	-	-	-	-	
		@	h_{FE}	No Change	40	No Change	-	-	-	-	
		-2.5V	I_{EBO}	No Change	No Change	No Change	-	-	-	-	
5	43	8μA	Parameters / Tests	50 zaps @ ± 7KV	10 zaps @ ± 7 KV	70 zaps @ ± 7KV	-	-	-	-	
		@	h_{FE}	No Change	40	No Change	-	-	-	-	
		-2.5V	I_{EBO}	No Change	No Change	No Change	-	-	-	-	

DEVICE UNDER TEST: ENI 14B RF POWER TRANSISTOR SB

TABLE 2

Sample No.	Measured Rezap Data a		ESD - Human Body Model Zap Tests & Results							Comments	Remarks
			Test Sequences								
	h_{FE} @ 80 MA	I_{EBO}	Parameters / Tests	b	c	d	e	f	g		
1	44	2 μA @ -2V		5 zaps @ -50V to -5 KV (Assorted)	5 zaps @ -16KV	25 zaps @ -16 KV	70 zaps @ -16KV	20 zaps @ +16KV	40 zaps @ +16KV	-	1. For all the devices zaps are applied between Base and Emitter unless otherwise specified.
			h_{FE}	No change	No change	No change	No change	34	No change		
			I_{EBO}	No change	5.2μA	7.5μA	8μA	No change	No change		
2	56	130μA @ -2V	Parameters / Tests	5 zaps @ -50V to -16KV (Assorted)	5 zaps @ -16KV	10 zaps @ -16KV	30 zaps @ +16KV	10 zaps @ -16KV	-	-	
			h_{FE}	54.5	53	53	No change	No change	-		
			I_{EBO}	170μA	200μA	250μA	No change	No change	-		
3	55	1.8μA @ -3V	Parameters / Tests	5 zaps @ -50V to -16KV (Assorted)	35 zaps @ -16KV	15 zaps @ + 16KV	-	-	-	-	2. Relevant to the test sequences indicated the measured graphical data are presented in figs. B.1.a to B.4.e
			h_{FE}	No change	No change	No change	-	-	-		
			I_{EBO}	No change	No change	No change	-	-	-		
4	51	1.2μA @ -3V	Parameters / Tests	$5V_{CE}$ zaps @ +500V to +16KV	$10V_{CE}$ zaps @ +16KV	$5V_{CE}$ zaps @ -16KV	$20V_{CE}$ zaps @+16KV	-	-	-	
			h_{FE}	No change	No change	No change	No change	-	-		
			I_{EBO}	No change	No change	No change	No change	-	-		

DEVICE UNDER TEST: ENI 2240 RF POWER TRANSISTOR #C

TABLE 3

Sample No.	Measured Prezap Data @				ESD - Human Body Model Zap Tests & Results						Comments	Remarks
					Test Sequences							
	h_{FE} @ 80 MA	I_{EBO}	$V_{CE\ sat}$	R_E+R_B Contact Resistance	b	c	d	e	f	g		
1	49.4	6 μA @ -2.5V	0.7V @ 80 MA 0.5V @ 20 MA	Not measured (Marginal)	Parameters / Tests	90 Zaps @ ± 7KV	65 zaps @ + 16KV	15 zaps @ + 16 KV	7 zaps @ + 16 KV	2 zaps @ + 16KV	-	Catastrophic damage due to metallic path formation between Base and collectors	1 All zaps are applied between Base and Emitter unless otherwise specified.
					h_{FE}	No change	48.6	? I_{cmax}=65 MA	? I_{cmax}=25MA	?	-		
					I_{EBO}	No change	No change	5.6 μA	5.3 μA	1 μA	-		
					$V_{CE\ sat}$	No change	1.1V @ 80 MA 0.5V @ 20MA	? 0.9 @ 20 MA	? 1.4V @ 20 MA	? ?	-		
					(R_E+R_B)	Not measured	Not measured	20 ohms	45 ohms	700 ohm	-		
2	48.6	6.8 μA @ -2.5V	0.7V @ 80 MA 0.5V @ 20 MA	Not measured (Marginal)	Parameters / Tests	5 zaps @ -50V to -16KV Assorted	25 zaps @ ± 16 KV	30 zaps @ ± 16 KV	-	-	-		2 Relevant to the test sequenced indicated measures graphical data are shown in Figs. C.1.a to C.3.c.
					h_{FE}	No change	No change	Catastrophic Damage	-	-	-		
					I_{EBO}	No change	No change	-do-	-	-	-		
					$V_{CE\ sat}$	No change	0.9V @ 80MA 0.5V @ 20MA	-do-	-	-	-		
					(R_E+R_B)	Not measured	Not measured	-do-	-	-	-		
3	35 @ 70 MA	15 μA @ -2.5V	0.8V @ 70 MA	Not measured (Marginal)	Parameters / Tests	40 V_{CE} zaps @ + 7KV	50 V_{CE} zaps @ +16 KV	-	-	-	-		
					h_{FE}	No change	?	-	-	-	-		
					I_{EBO}	-do-	No change	-	-	-	-		
					$V_{CE\ sat}$	-do-	?	-	-	-	-		
					(R_E+R_B)	-do-	Stays marginal	-	-	-	-		

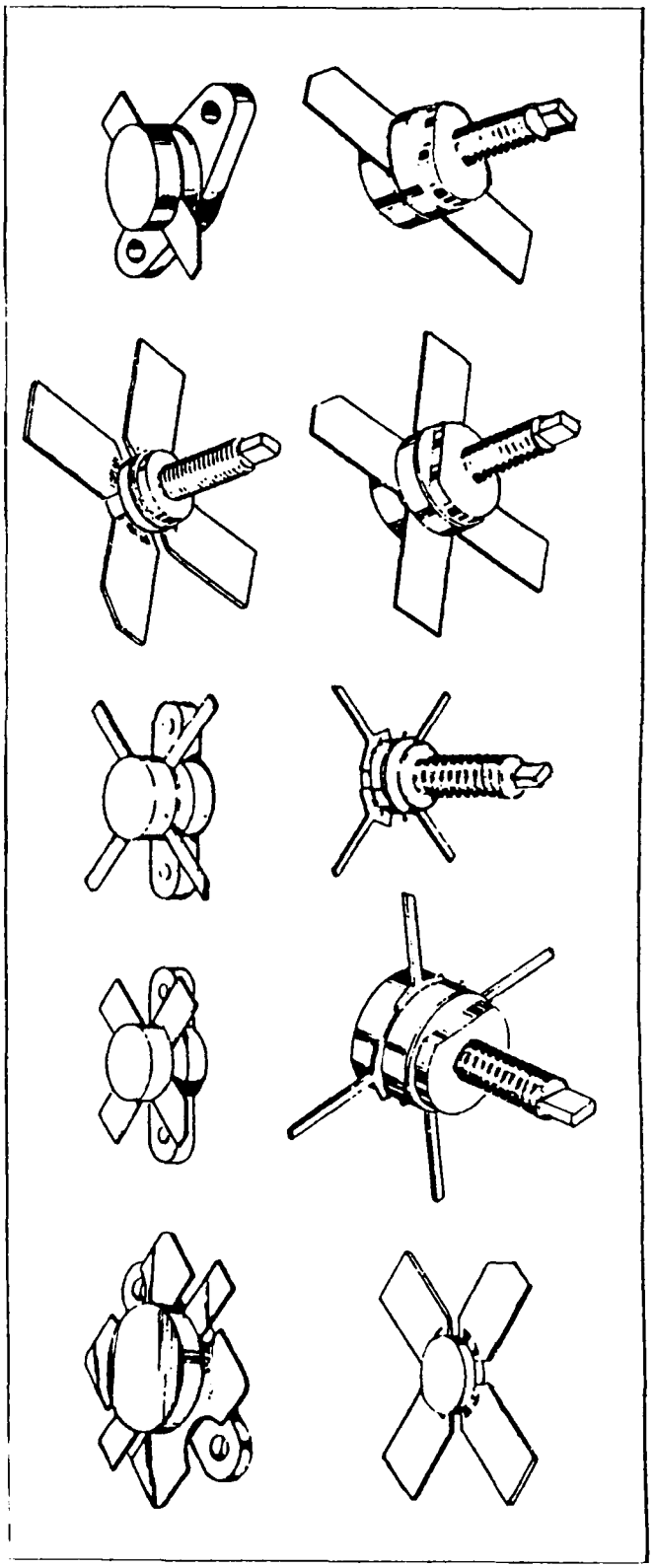


FIGURE 1 – SOE Packages

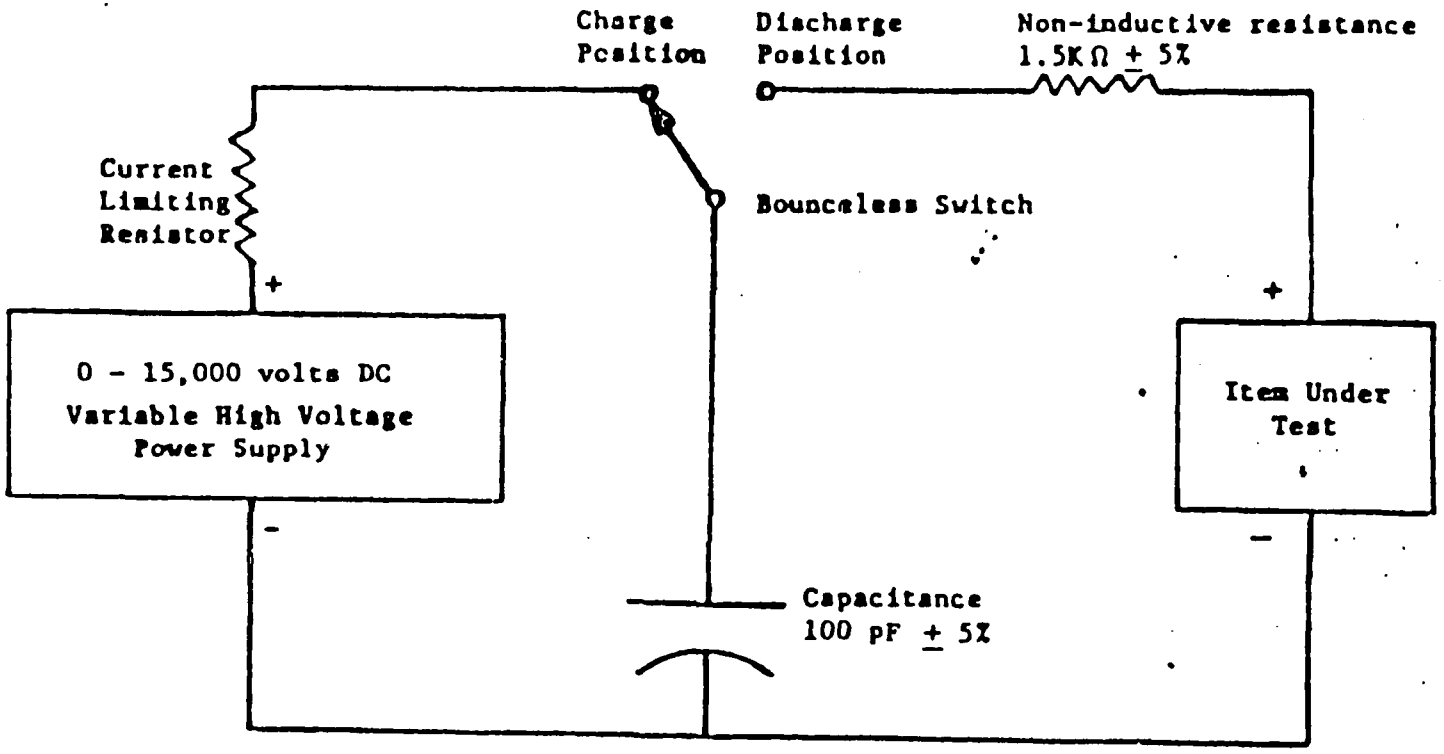
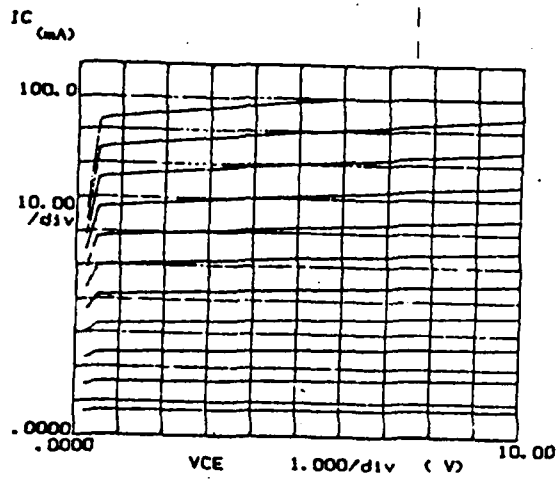


FIGURE 2. ESD test circuit

NOTE: Test voltages are measured across the capacitance. The capacitor shall be discharged through the series resistor into the item under test by maintaining the bounceless switch to the discharge position for a time no shorter than required to decay the capacitor voltage to less than 1 percent of the test voltage or 5 seconds, whichever is less. Power supply voltage shall be within a tolerance of ±5 percent of test voltage.

Figs. A.1.a

****** GRAPHICS PLOT ******

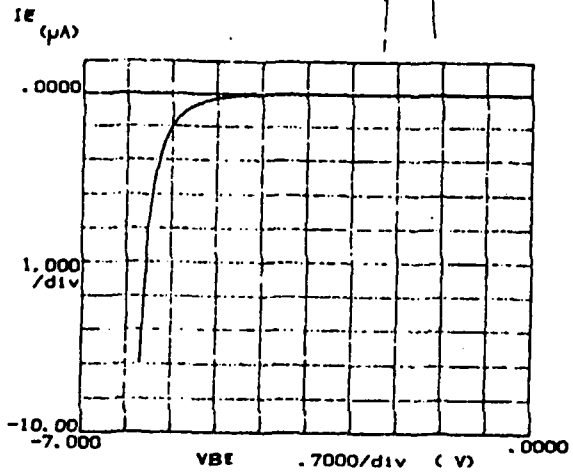


Variable1:
VCE -Ch0
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable0:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constant:
VE -Ch1 .0000V

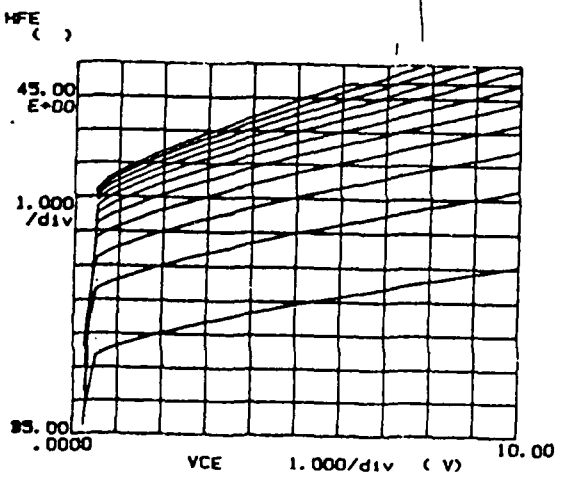
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -7.0000V
Step -.0450V

Constant:
V -Ch3 .0000V

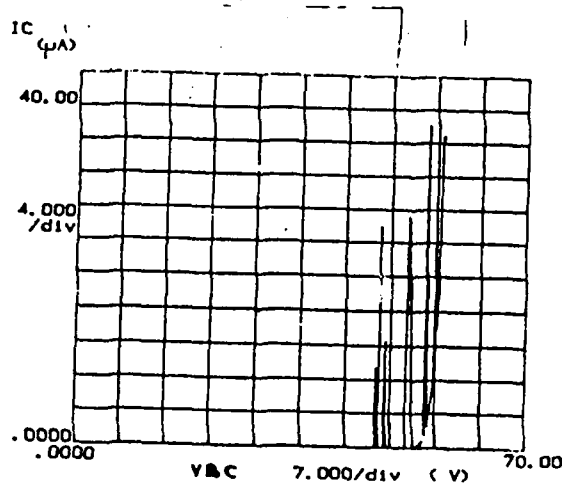
****** GRAPHICS PLOT ******



Variable1:
VCE -Ch0
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable0:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constant:
VE -Ch1 .0000V



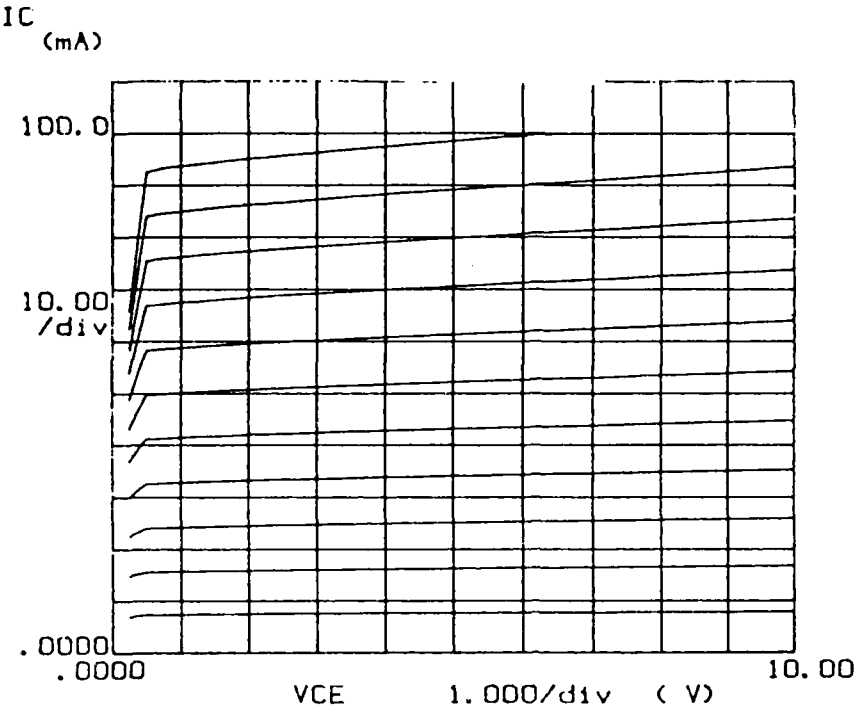
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Linear sweep
Start .0000V
Stop 70.000V
Step .2000V

Variable0:
IB -Ch2
Start .000 A
Stop .000 A
Step .000 A

Constant:
VE -Ch1 .0000V

Figs. A.1.b

****** GRAPHICS PLOT ******



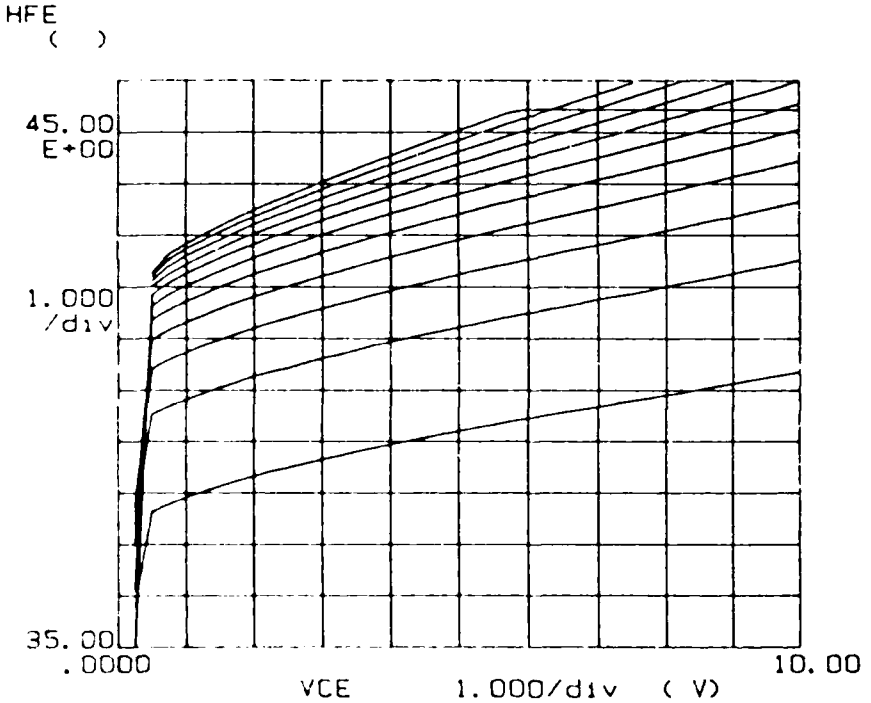
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

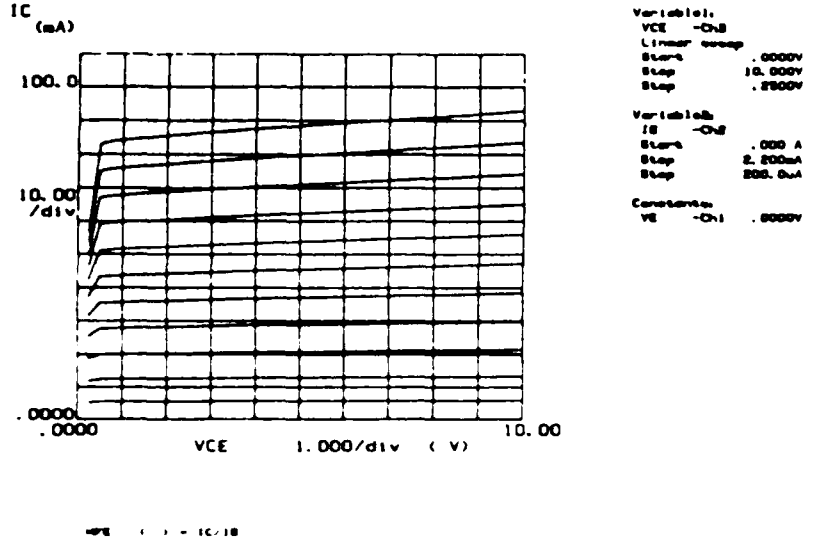
Variable2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

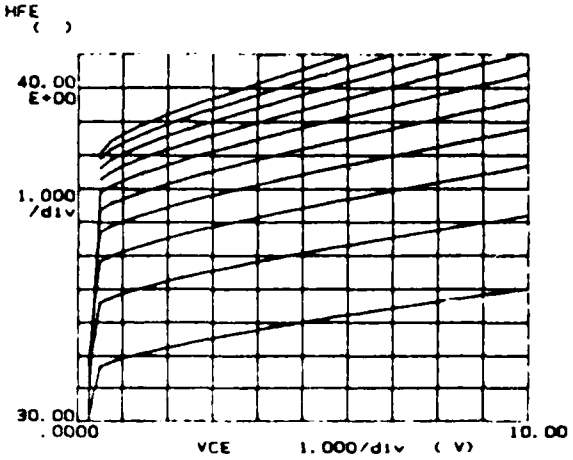
HFE ( ) = IC/IB

Figs. A.1.c

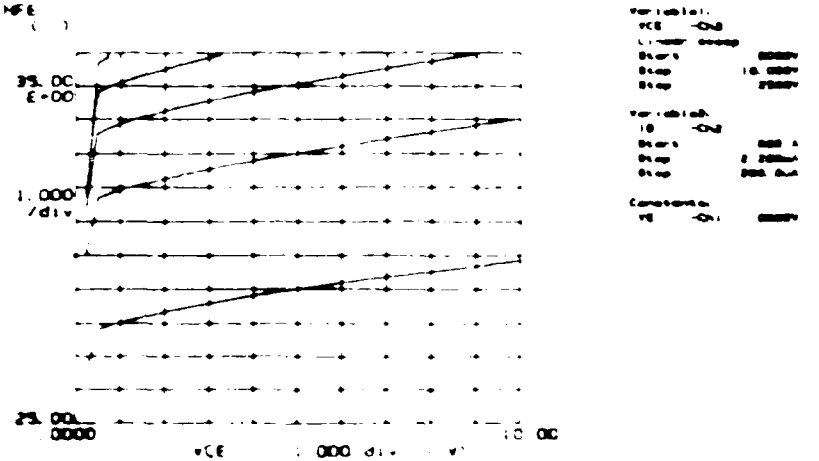
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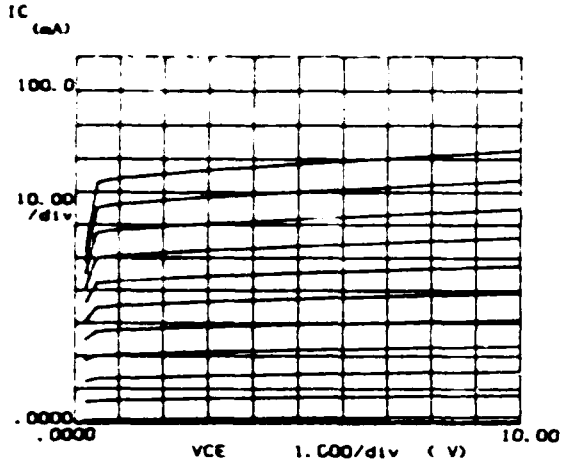


****** GRAPHICS PLOT ******



Figs. A.1.1

****** GRAPHICS PLOT ******



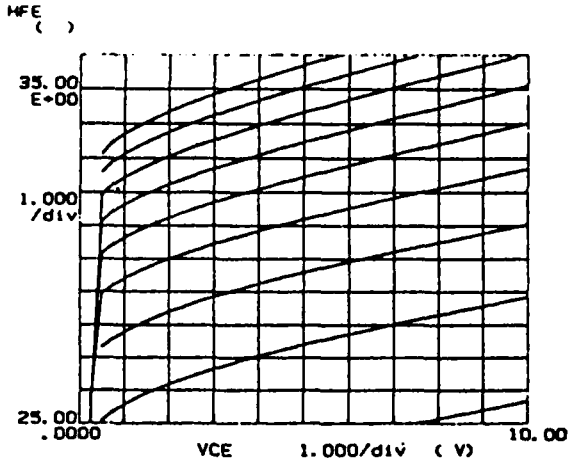
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

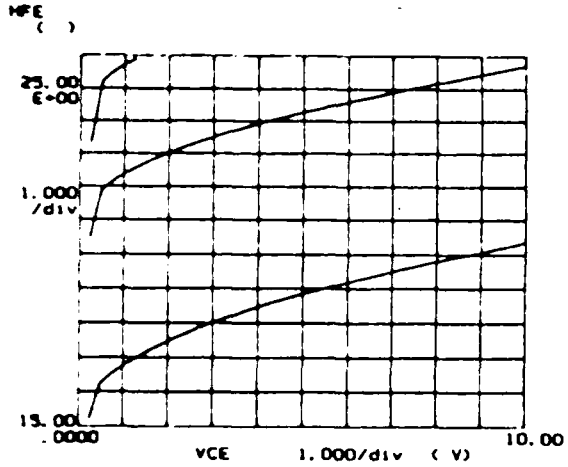
Variable2:
IB -Ch2
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

-96-

****** GRAPHICS PLOT ******



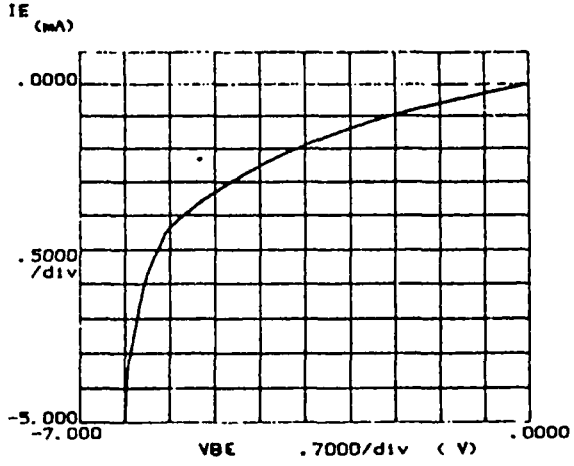
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

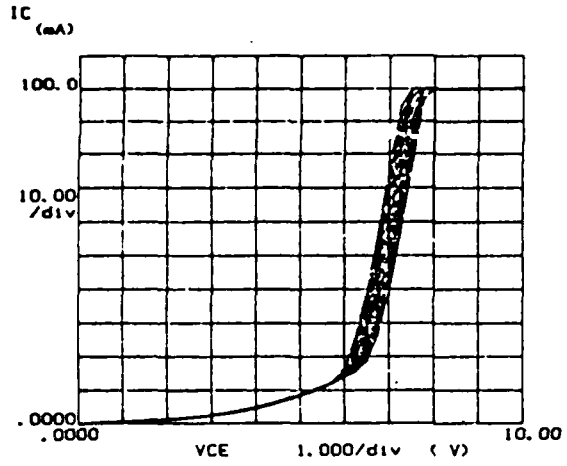


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -7.0000V
Step -.0450V

Constants:
V -Ch2 .0000V

Figs. A.1.e

****** GRAPHICS PLOT ******



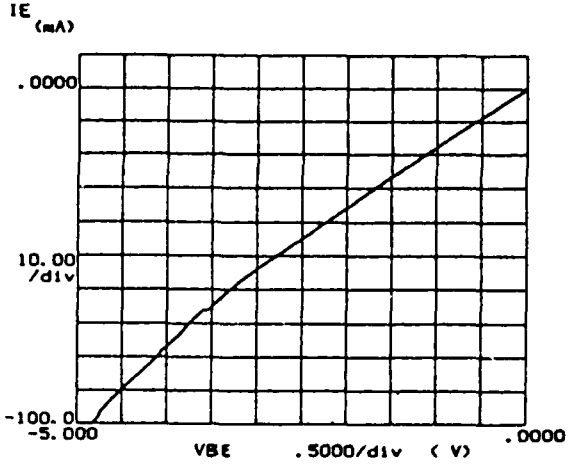
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Step 10.000V
Stop .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.200mA
Stop 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

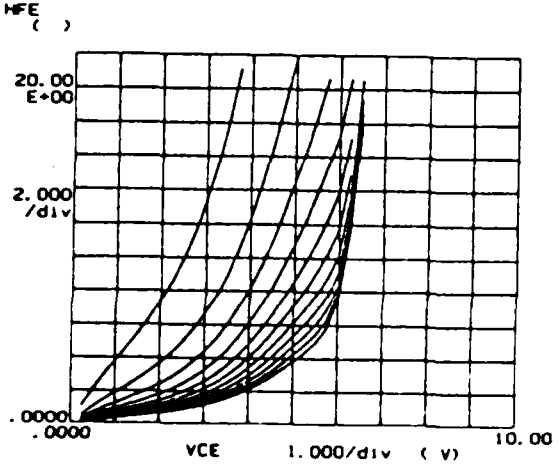
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -5.0000V
Stop -.0450V

Constants:
V -Ch2 .0000V

****** GRAPHICS PLOT ******



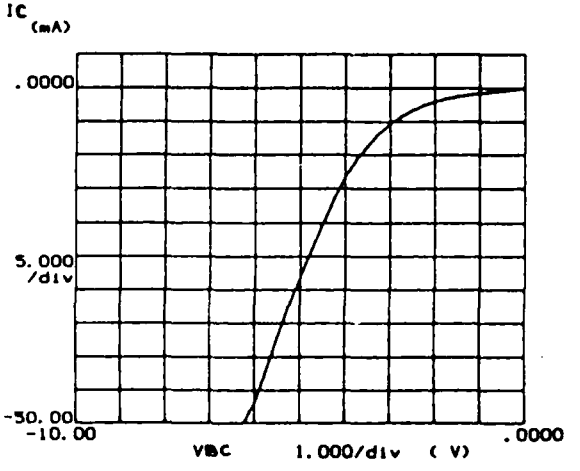
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Step 10.000V
Stop .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.200mA
Stop 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

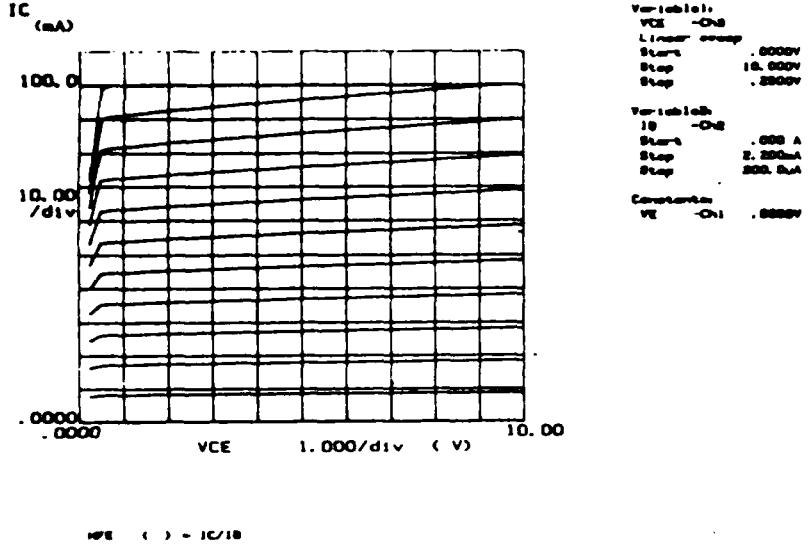


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -10.000V
Stop -.2500V

Constants:
V -Ch2 .0000V

Figs. A.2.a

****** GRAPHICS PLOT ******



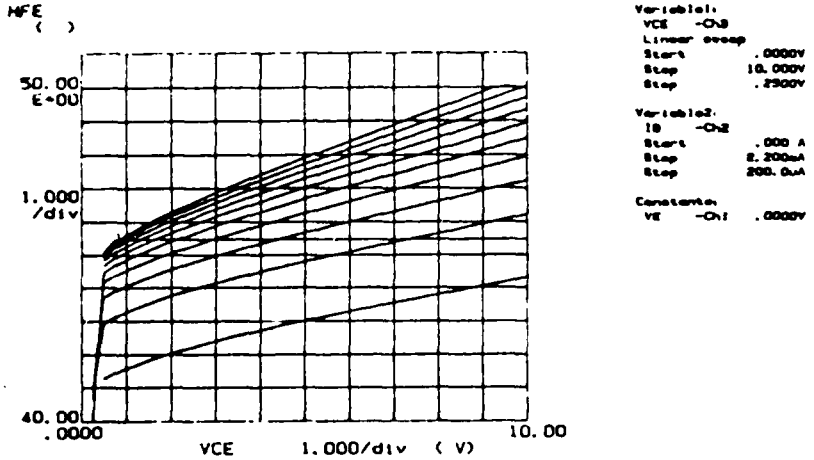
Variable1:
VCE -Ch0
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



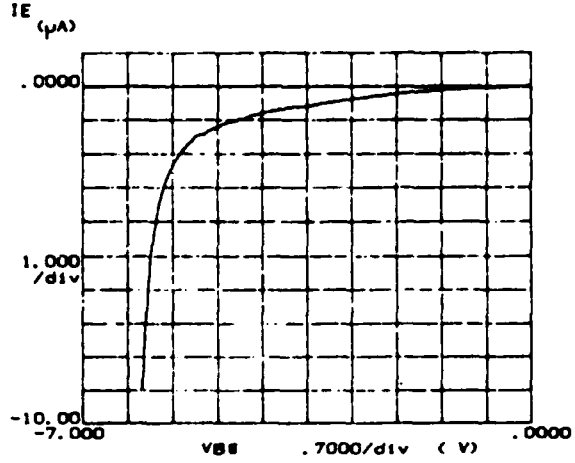
Variable1:
VCE -Ch0
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

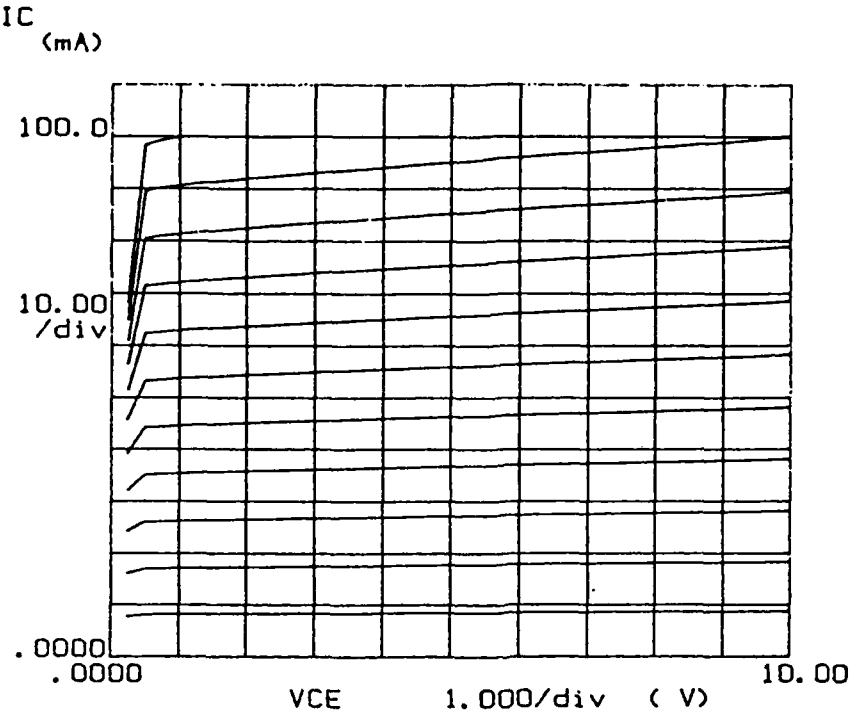


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -7.0000V
Step -.0450V

Constants:
V -Ch0 .0000V

Figs. A.2.b

****** GRAPHICS PLOT ******



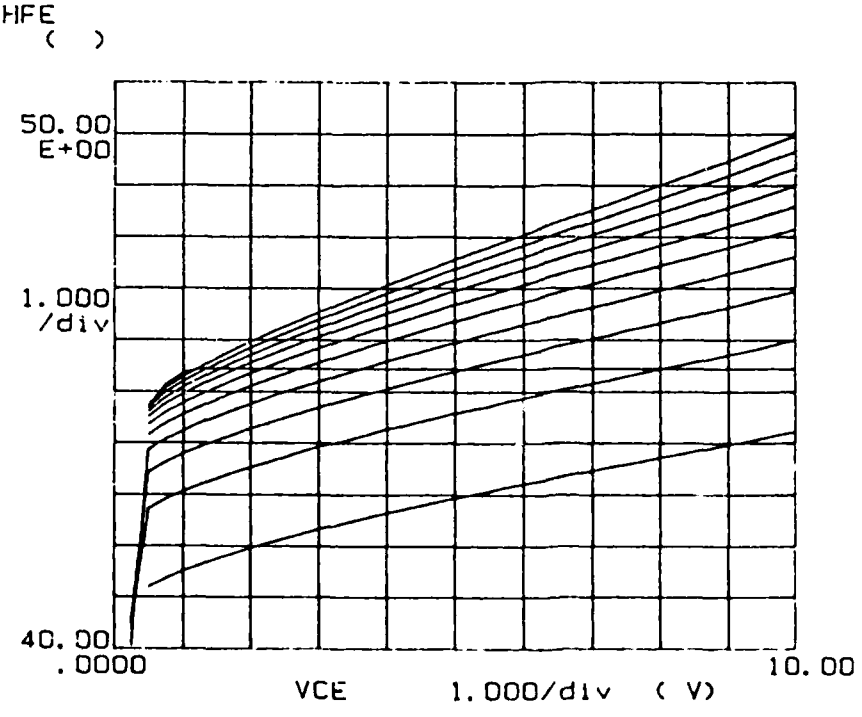
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

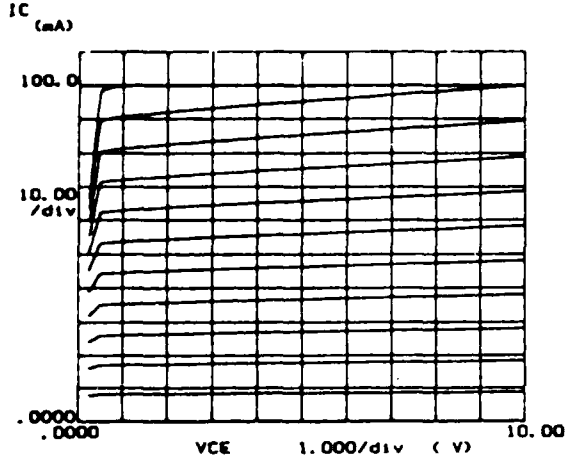
Variable2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

Figs. A.2.c

****** GRAPHICS PLOT ******



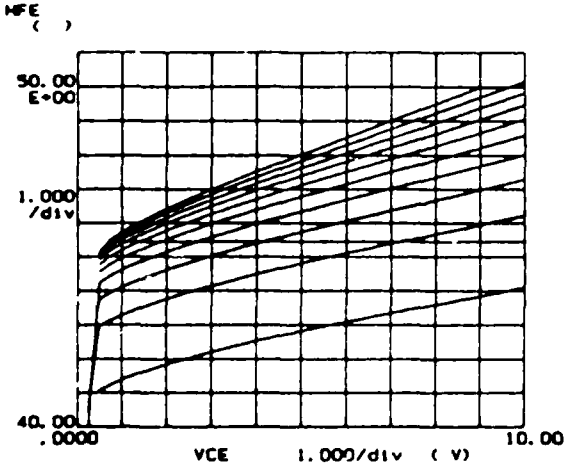
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



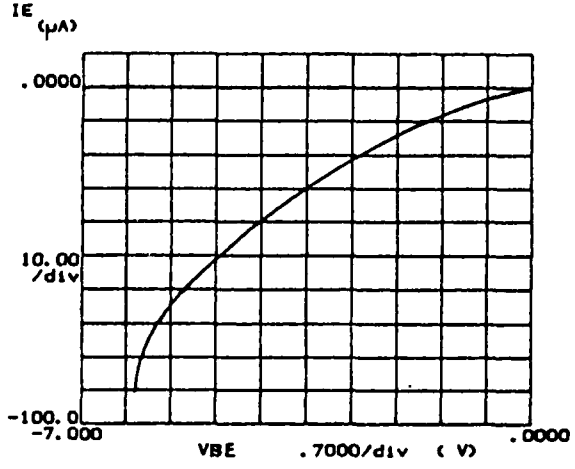
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

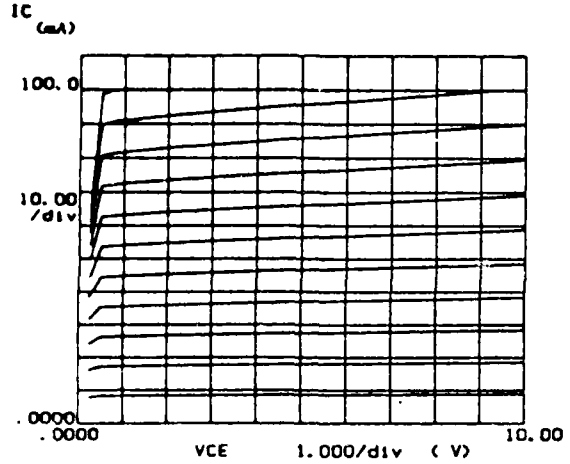


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -7.0000V
Step -.0490V

Constants:
V -Ch2 .0000V

Figs. A.2.d

****** GRAPHICS PLOT ******



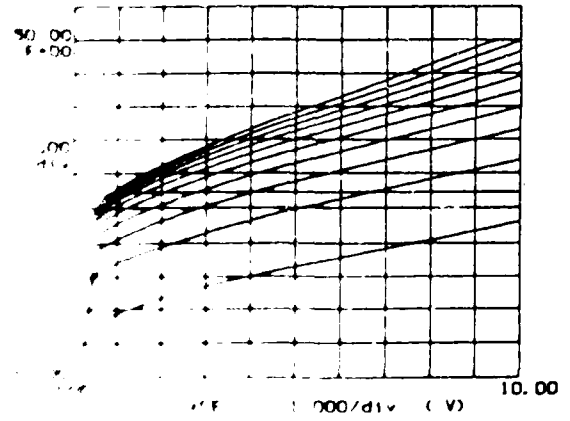
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

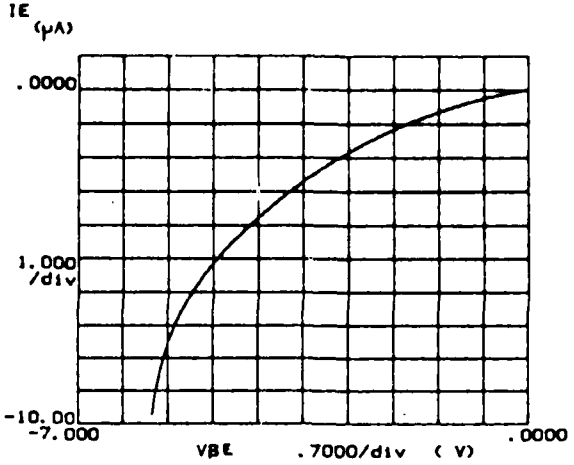


Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

****** GRAPHICS PLOT ******



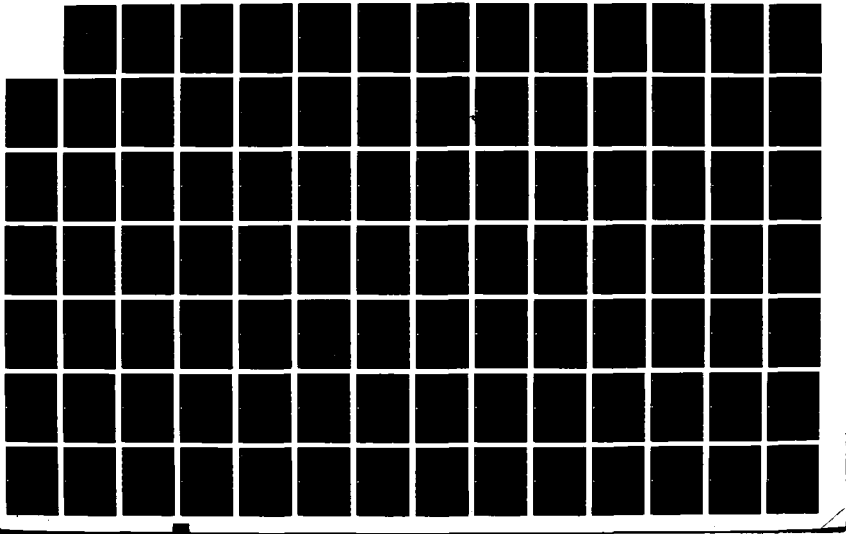
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -7.0000V
Step -.8750V

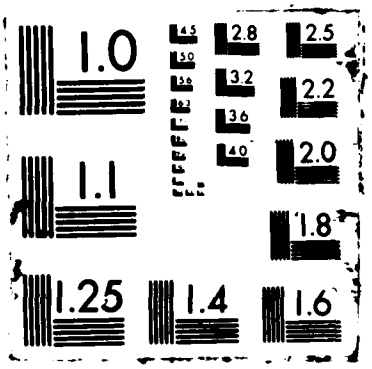
Constants:
V -Ch3 .0000V

AD-A184 906 ELECTROMAGNETICS AND ELECTROTHERMAL APPROACH TO EVALUATE FAILURES IN MICR..(U) RIT RESEARCH CORP ROCHESTER NY P S NEELAKANTASWAMY AUG 87 RITRC-014

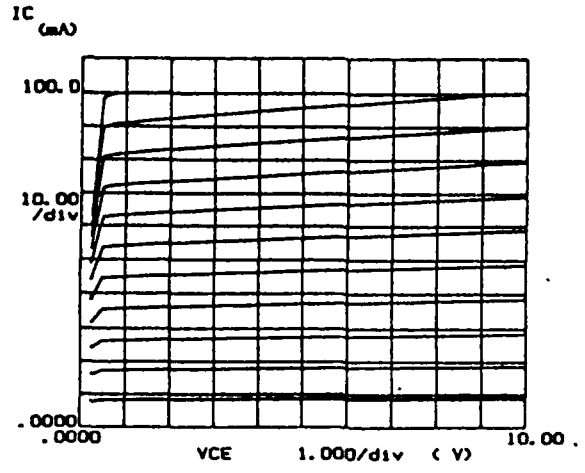
2/1

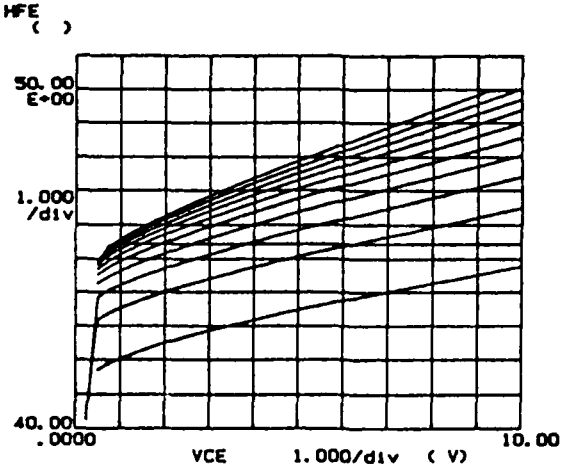
UNCLASSIFIED N00014-84-K-0532 F/G 20/3 NL

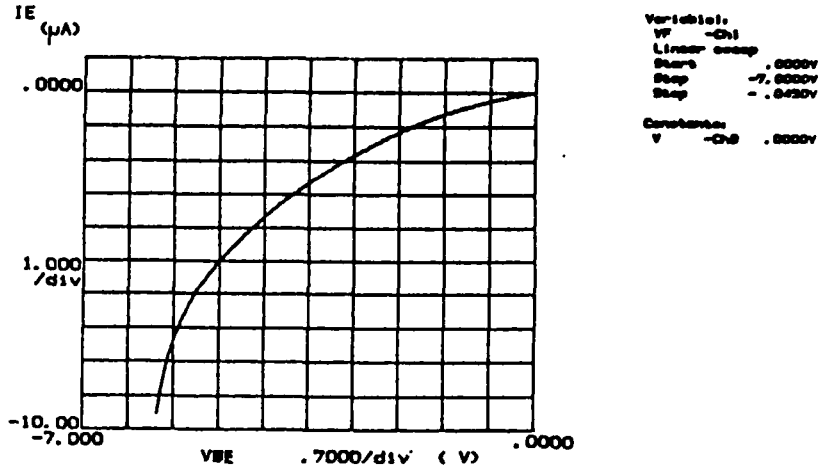



1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0

Figs. A.2.e

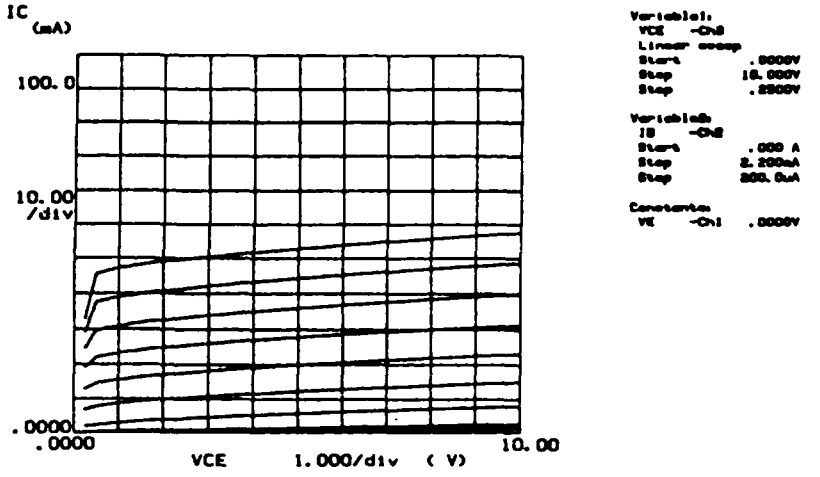

****** GRAPHICS PLOT ******
IC (mA)
100.0
10.00 /div
.0000
.0000
10.00
VCE 1.000/div (V)
Variable1:
VCE -Ch0
Linear sweep
Start .0000V
Step 10.000V
Step .2500V
Variable0:
IB -Ch2
Start .000 A
Step 2.200mA
Step 200.0uA
Constants:
VE -Ch1 .0000V
HFE ( ) = IC/IB


****** GRAPHICS PLOT ******
HFE ( )
50.00 E+00
1.000 /div
40.00
.0000
10.00
VCE 1.000/div (V)
Variable1:
VCE -Ch0
Linear sweep
Start .0000V
Step 10.000V
Step .2500V
Variable0:
IB -Ch2
Start .000 A
Step 2.200mA
Step 200.0uA
Constants:
VE -Ch1 .0000V
HFE ( ) = IC/IB

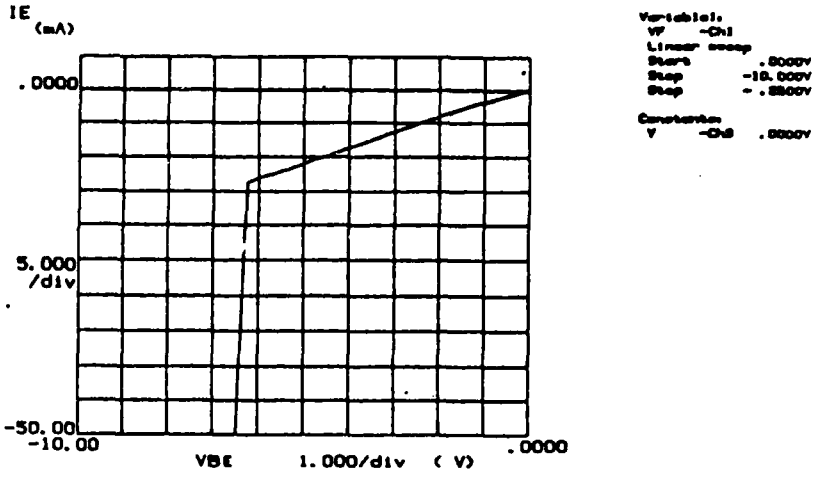

IE (μA)
.0000
1.000 /div
-10.00
-7.000
.0000
VBE .7000/div (V)
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -7.0000V
Step -.0420V
Constants:
V -Ch0 .0000V

Figs. A.2.f

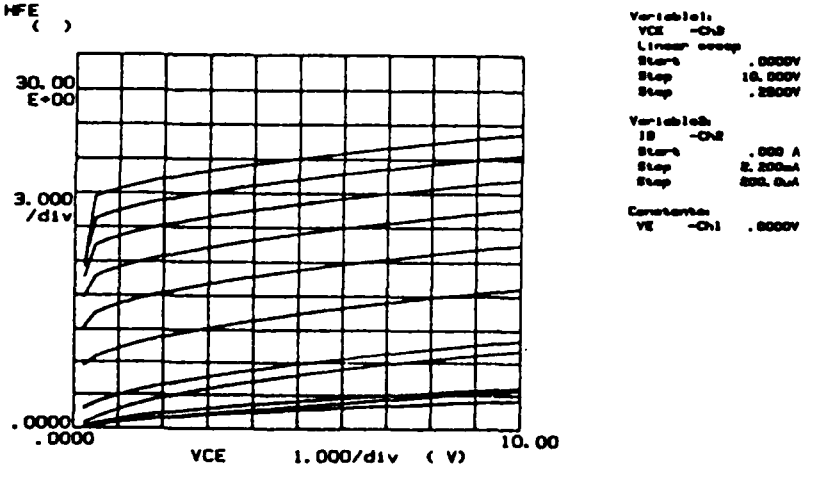
****** GRAPHICS PLOT ******



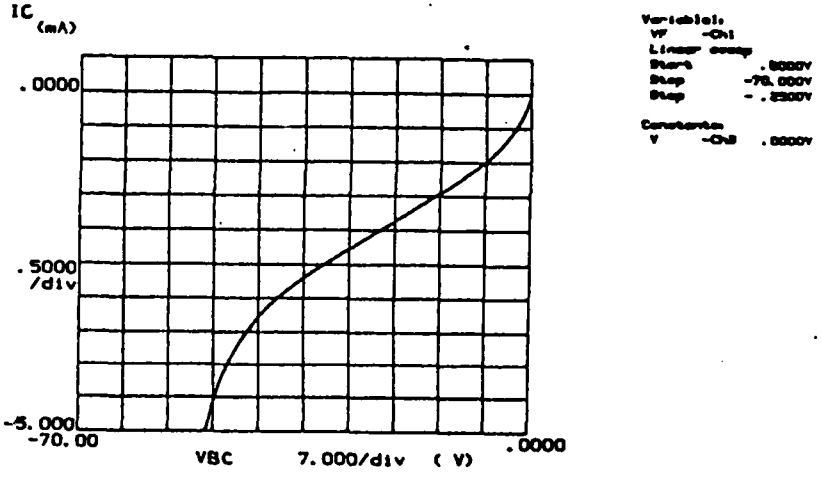
****** GRAPHICS PLOT ******



****** GRAPHICS PLOT ******

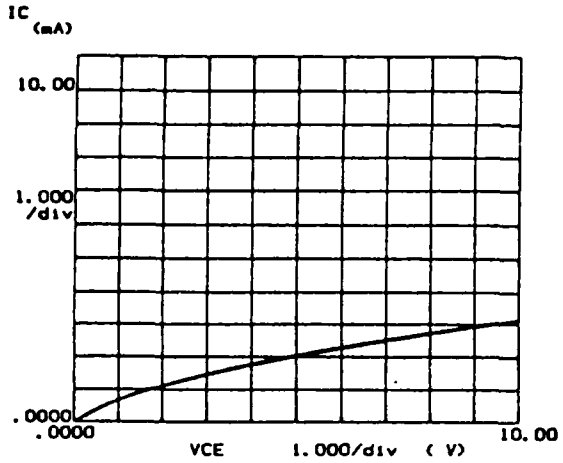


****** GRAPHICS PLOT ******



Figs. A.2.g

****** GRAPHICS PLOT ******



Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

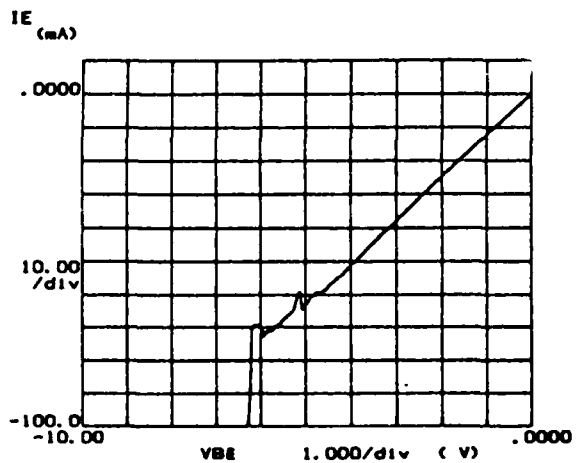
Variable2:
IB -Ch1
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

-42-

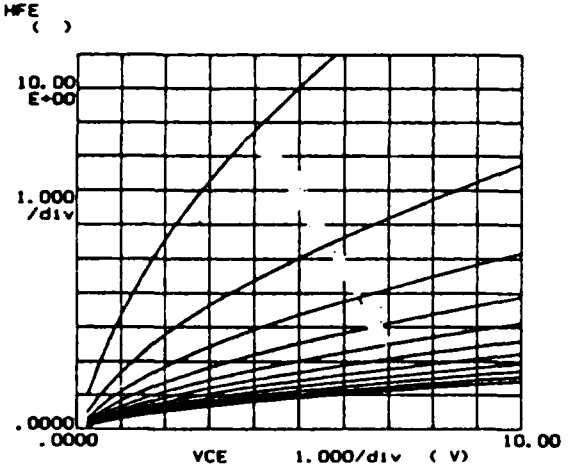
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -10.000V
Step -.0450V

Constants:
V -Ch2 .0000V

****** GRAPHICS PLOT ******



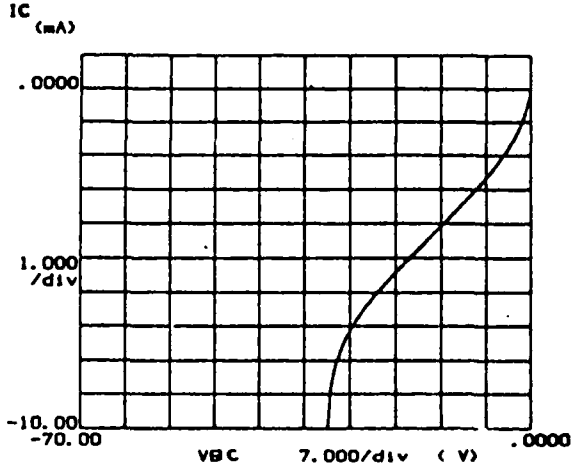
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch1
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

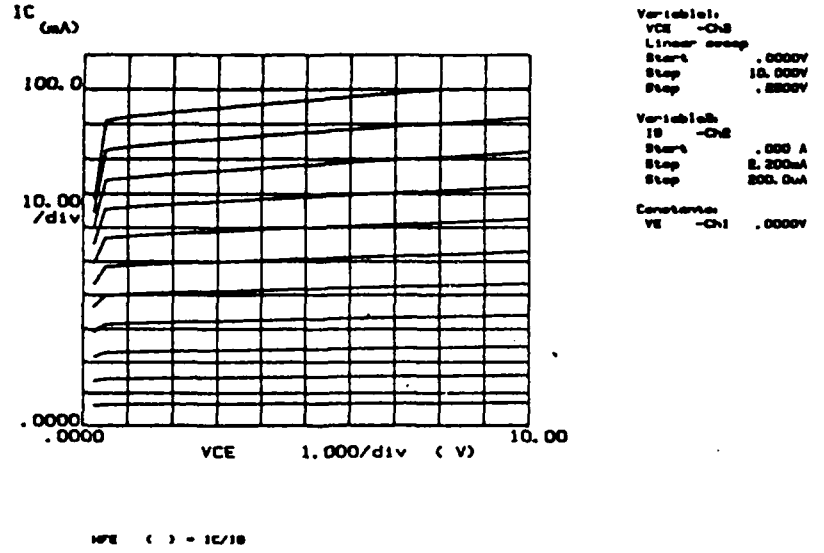


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -70.000V
Step -.3500V

Constants:
V -Ch2 .0000V

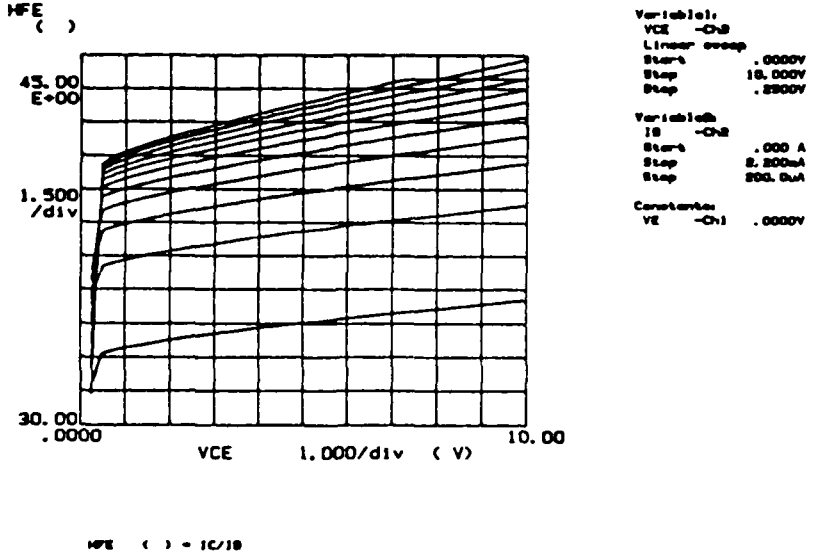
Figs. A.3.a

****** GRAPHICS PLOT ******



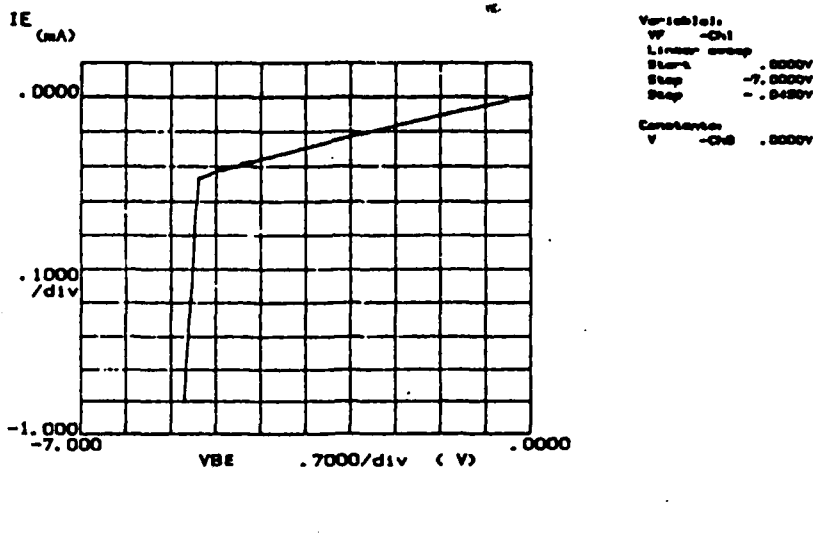
HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



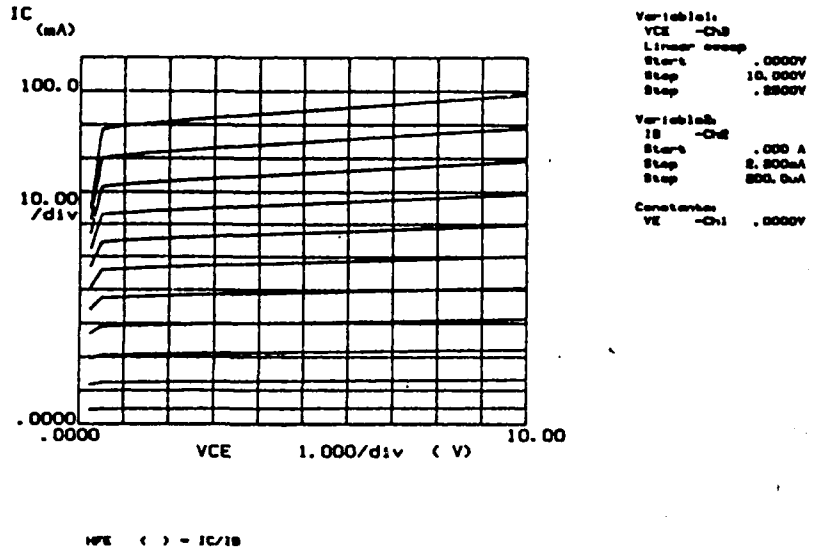
HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



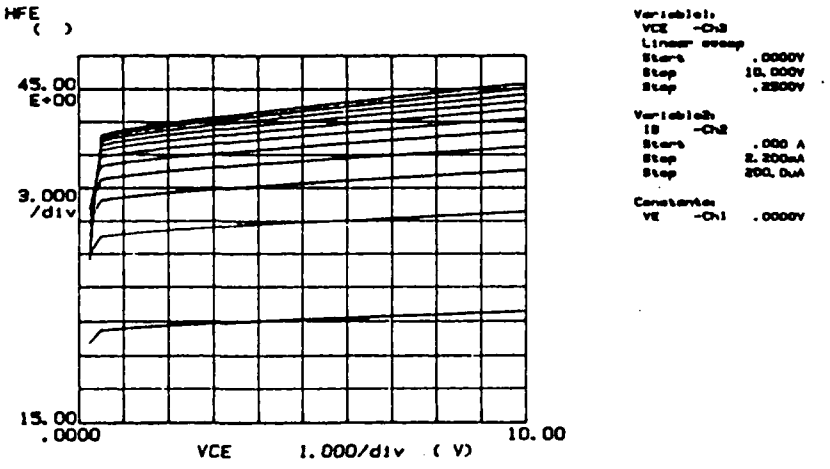
Figs. A.3.b

****** GRAPHICS PLOT ******



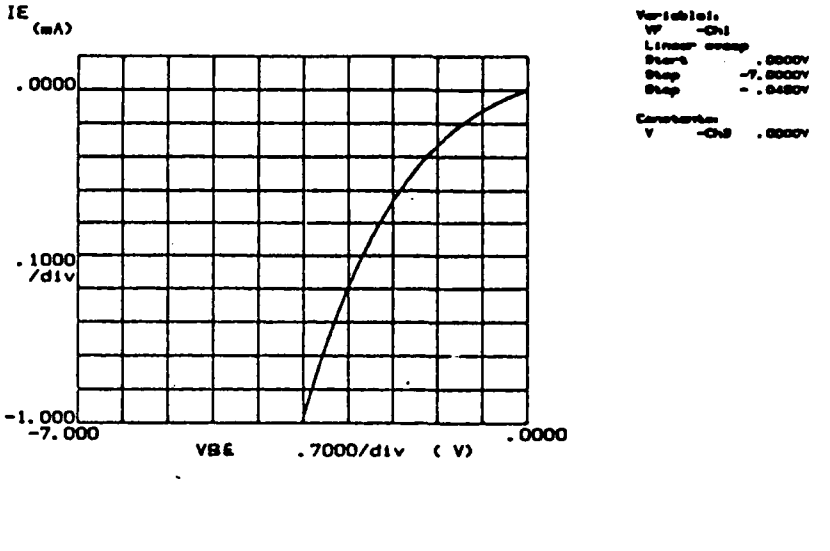
HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

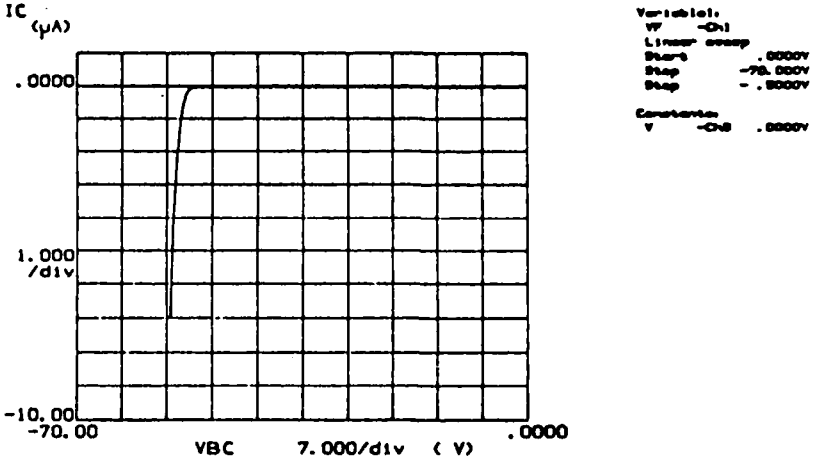


HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

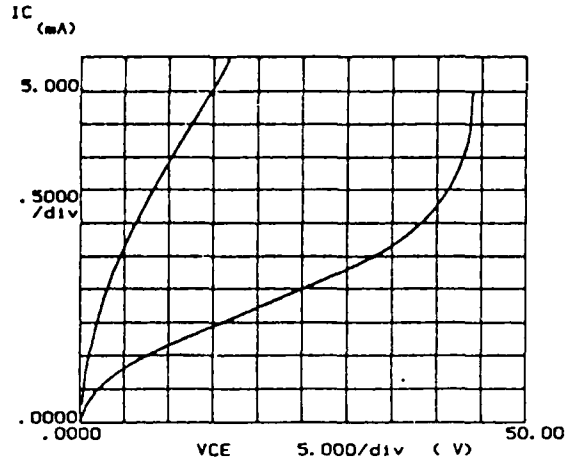


****** GRAPHICS PLOT ******



Figs. A.3.c

****** GRAPHICS PLOT ******



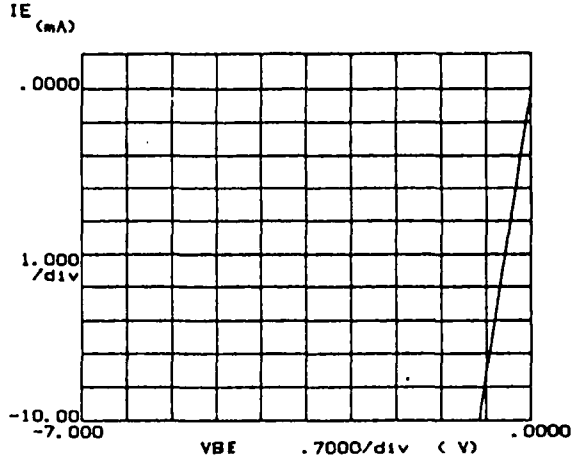
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Stop 50.000V
Step .2500V

Variable2:
IB -Ch1
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

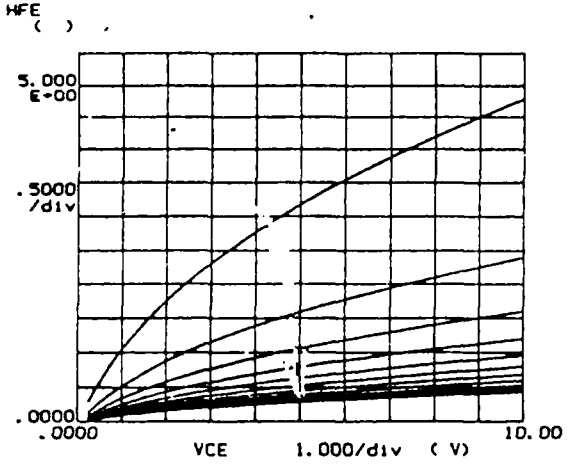
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -7.0000V
Step -.0450V

Constants:
V -Ch2 .0000V

****** GRAPHICS PLOT ******



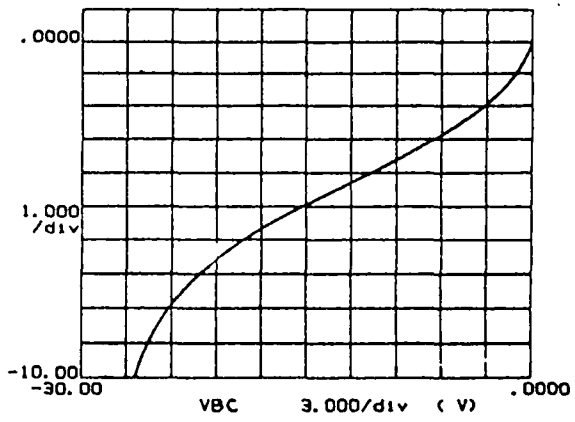
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch1
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

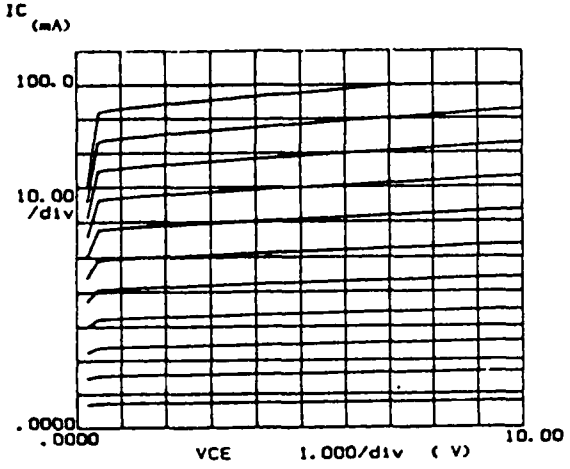


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -30.000V
Step -.1000V

Constants:
V -Ch2 .0000V

Figs. A.4.a

****** GRAPHICS PLOT ******



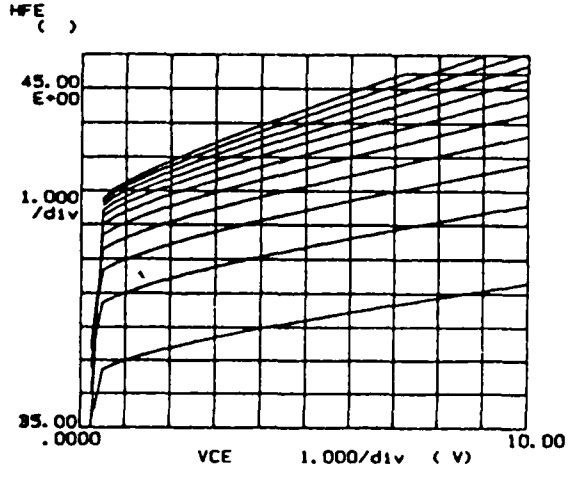
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch1
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



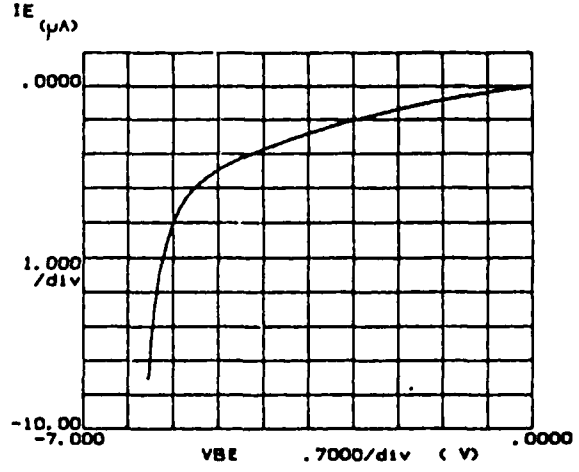
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch1
Start .000 A
Step 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

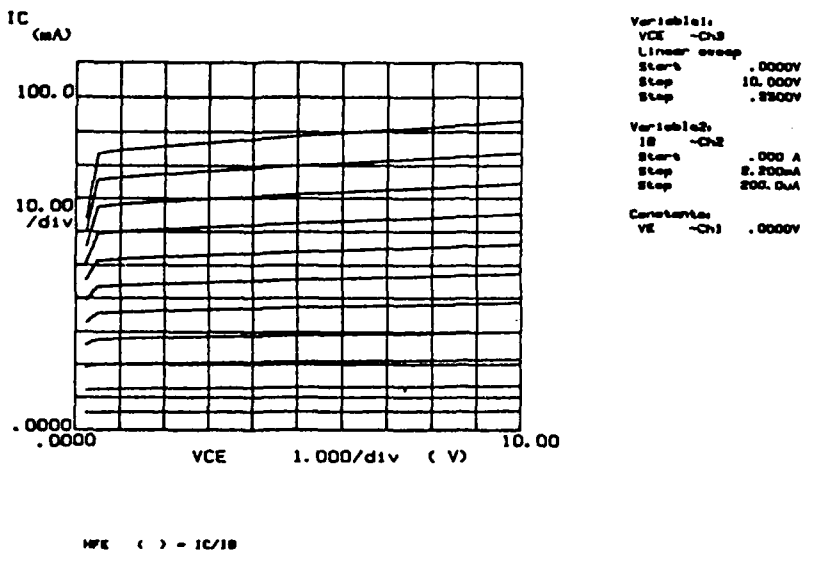
****** GRAPHICS PLOT ******

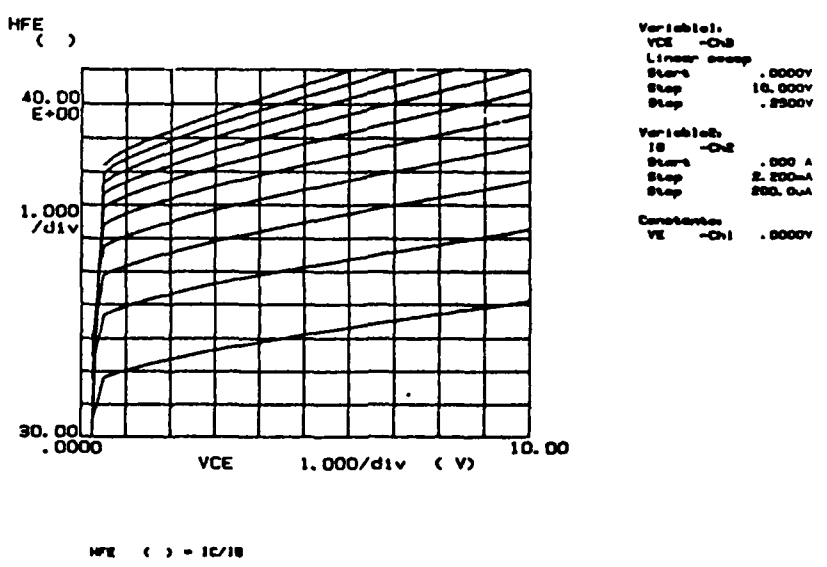


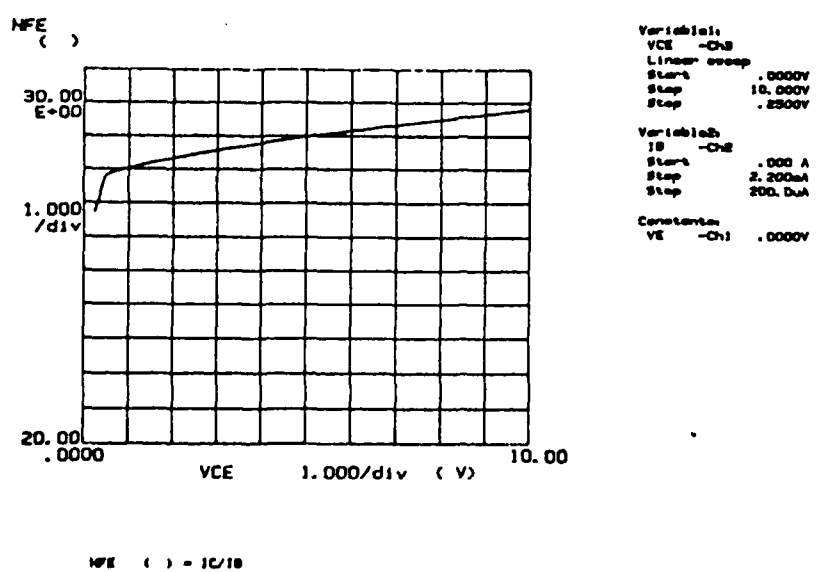
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -7.0000V
Step -.0450V

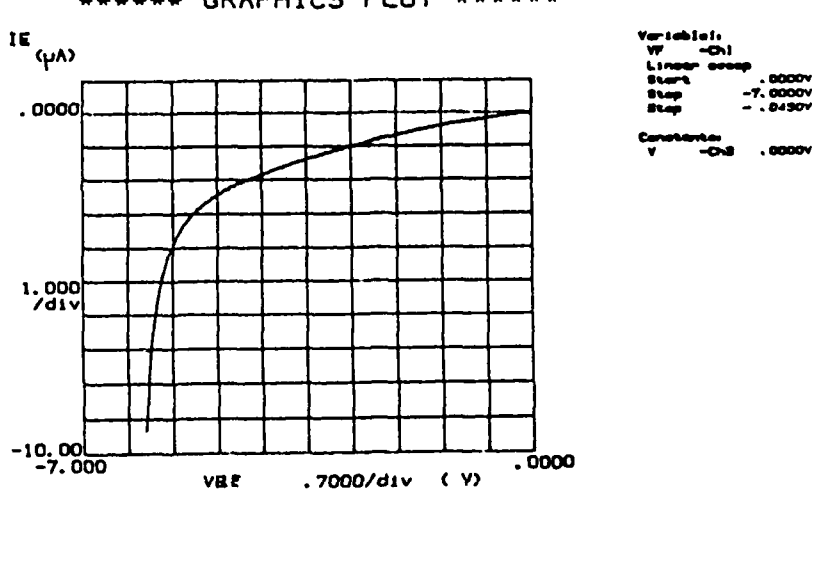
Constants:
V -Ch2 .0000V

Figs. A.4.c

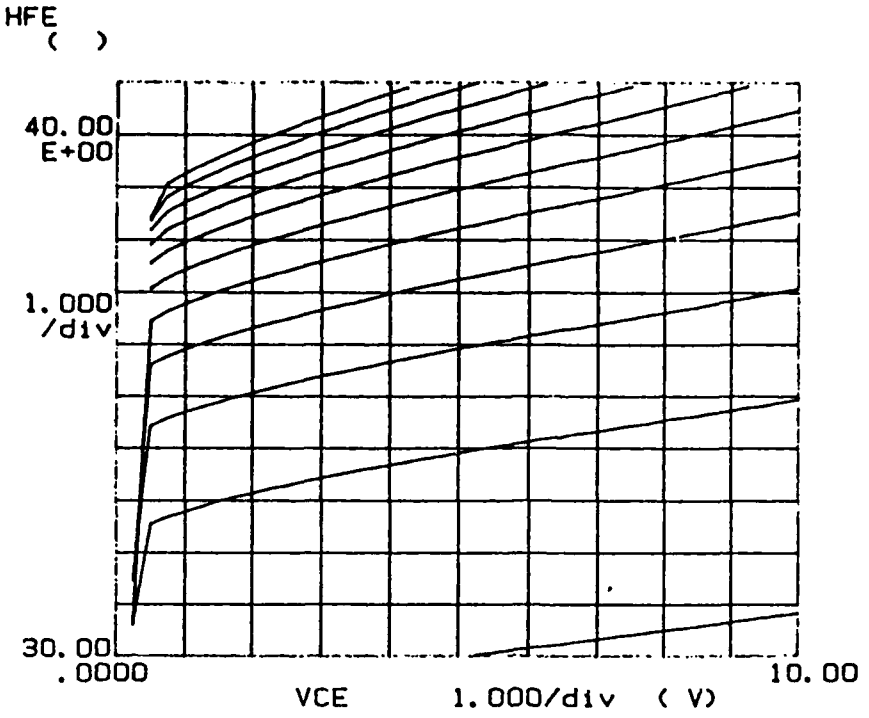

****** GRAPHICS PLOT ******
IC (mA)
100.0
10.00 /div
.0000
.0000
VCE 1.000/div (V)
10.00
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Step 10.000V
Stop .2500V
Variable2:
IB -Ch2
Start .000 A
Step 2.200mA
Stop 200.0uA
Constants:
VE -Ch1 .0000V
HFE ( ) = IC/IB


****** GRAPHICS PLOT ******
HFE ( )
40.00 E+00
1.000 /div
30.00
.0000
VCE 1.000/div (V)
10.00
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Step 10.000V
Stop .2500V
Variable2:
IB -Ch2
Start .000 A
Step 2.200mA
Stop 200.0uA
Constants:
VE -Ch1 .0000V
HFE ( ) = IC/IB


****** GRAPHICS PLOT ******
HFE ( )
30.00 E+00
1.000 /div
20.00
.0000
VCE 1.000/div (V)
10.00
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Step 10.000V
Stop .2500V
Variable2:
IB -Ch2
Start .000 A
Step 2.200mA
Stop 200.0uA
Constants:
VE -Ch1 .0000V
HFE ( ) = IC/IB


****** GRAPHICS PLOT ******
IE (μA)
.0000
1.000 /div
-10.00
-7.000
VBE .7000/div (V)
.0000
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -7.0000V
Stop -.0430V
Constants:
V -Ch3 .0000V

Figs. A.4.d



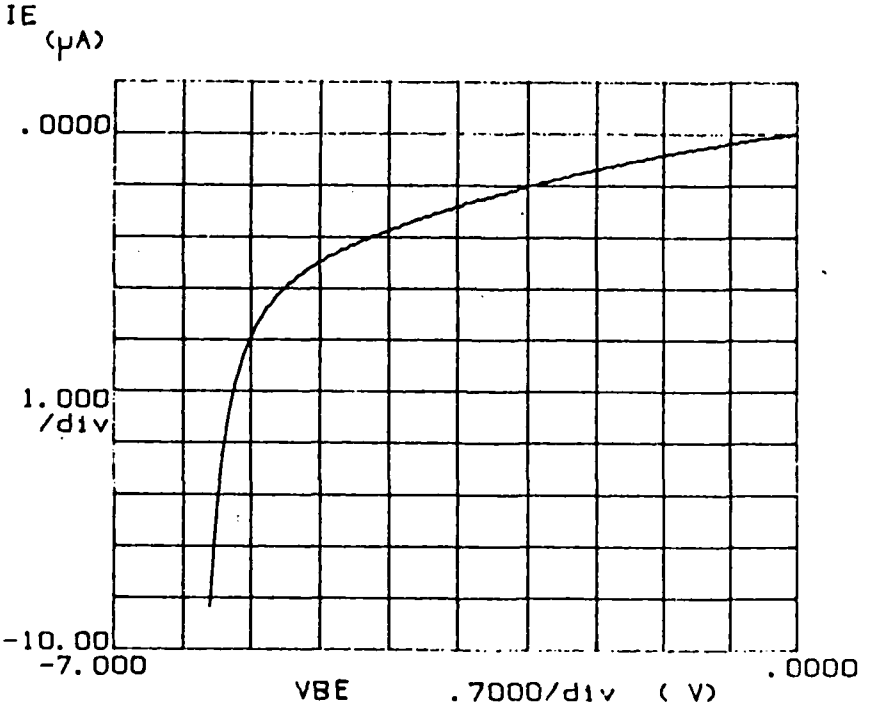
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

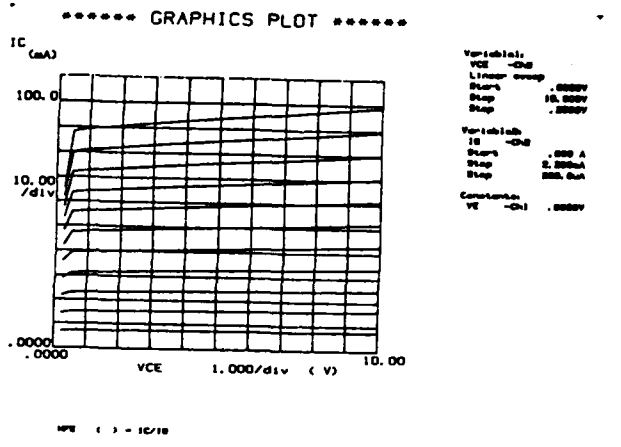
****** GRAPHICS PLOT ******

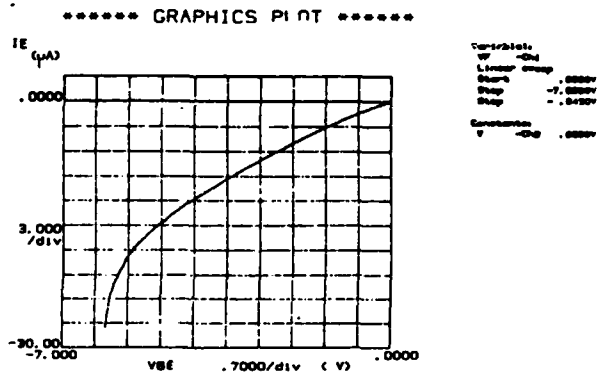


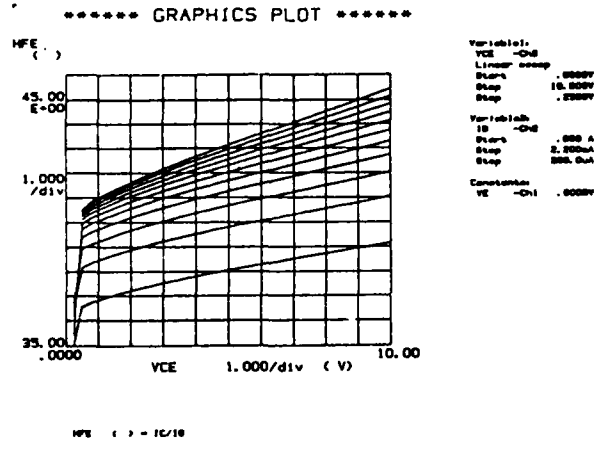
Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -7.0000V
Step -.0450V

Constants:
V -Ch3 .0000V

Figs. A.5.a

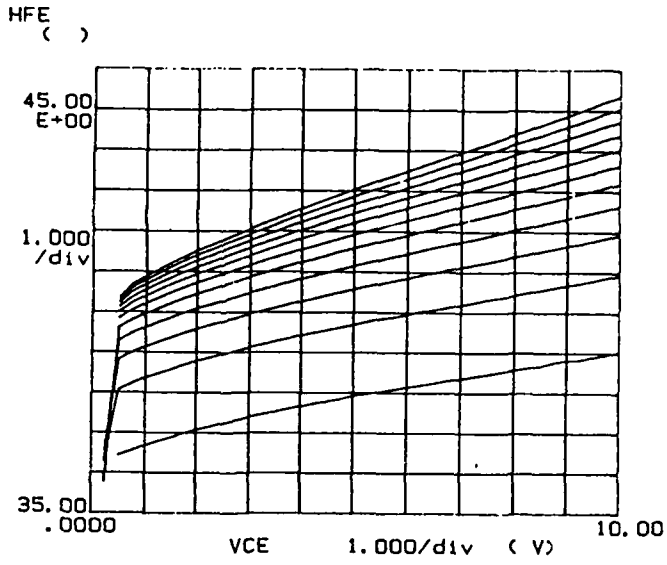

****** GRAPHICS PLOT ******
IC (mA)
100.0
10.00 /div
.0000
.0000
VCE 1.000/div (V)
10.00


****** GRAPHICS PLOT ******
IE (μA)
.0000
3.000 /div
-30.00
-7.000
VBE .7000/div (V)
.0000


****** GRAPHICS PLOT ******
HFE ( )
45.00 E+00
1.000 /div
35.00
.0000
VCE 1.000/div (V)
10.00

Figs. A.5.b

****** GRAPHICS PLOT ******



Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

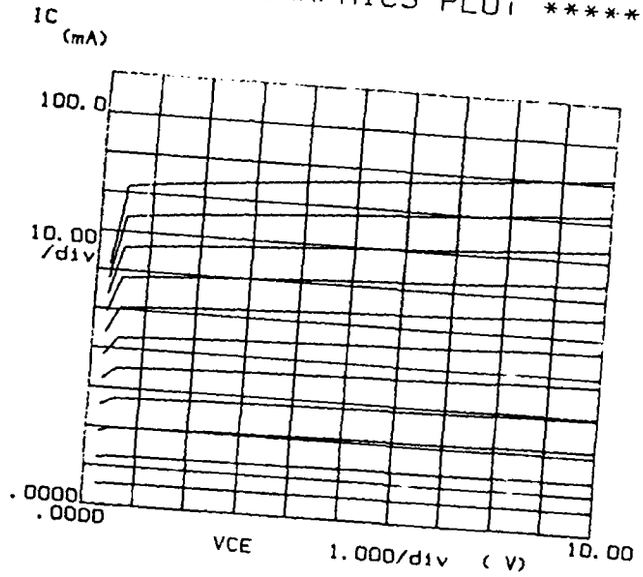
Variable2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

Figs. A.5.c

****** GRAPHICS PLOT ******



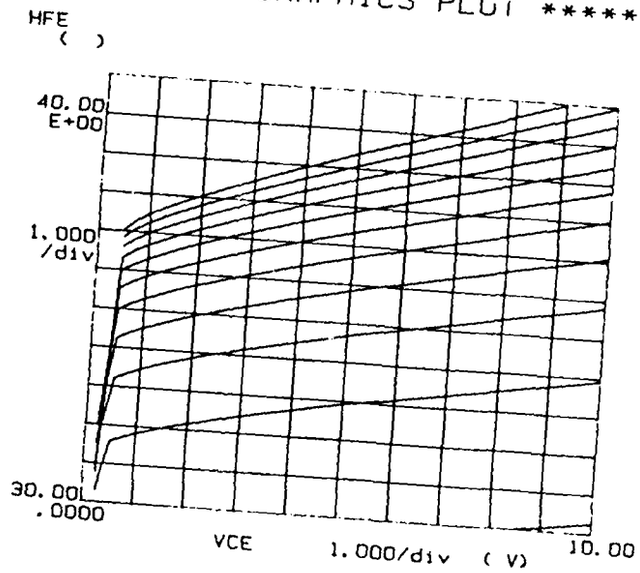
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

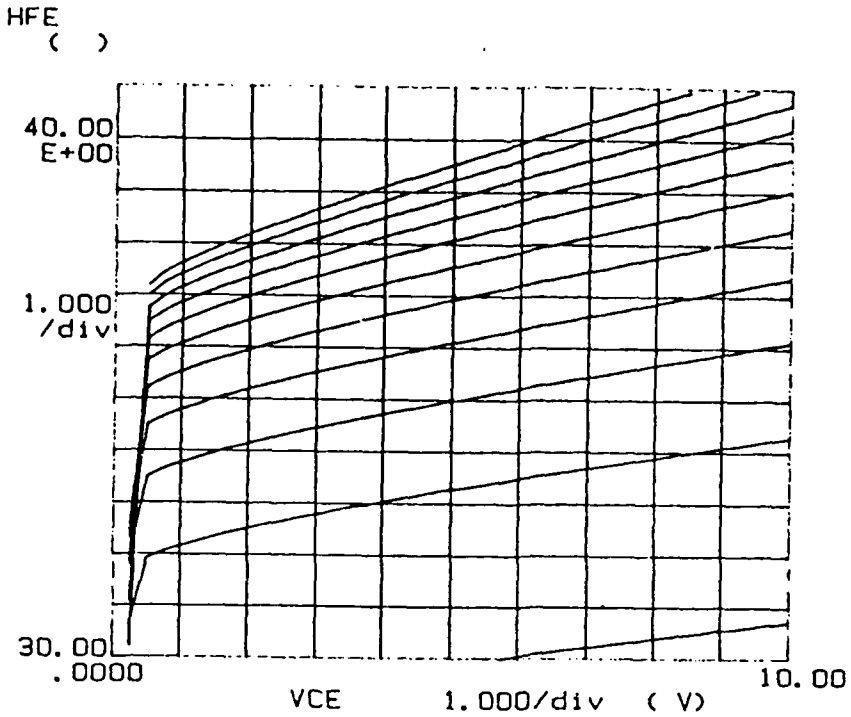
Variable2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

Figs. A.5.d

****** GRAPHICS PLOT ******



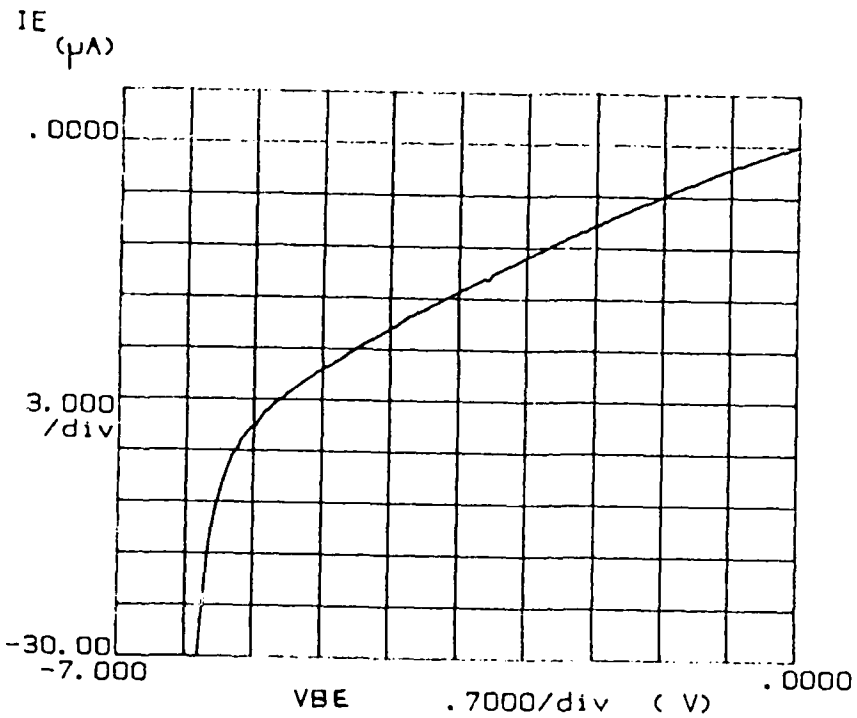
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Stop 2.200mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

***** GRAPHICS PLC ******

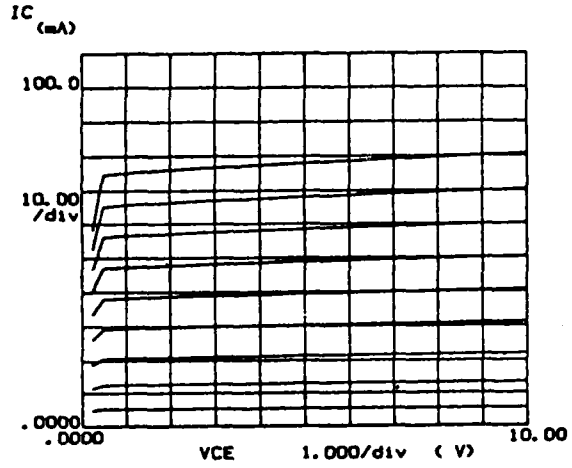


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -7.0000V
Step -.0450V

Constants:
V -Ch3 .0000V

Figs. B.1.a

****** GRAPHICS PLOT ******



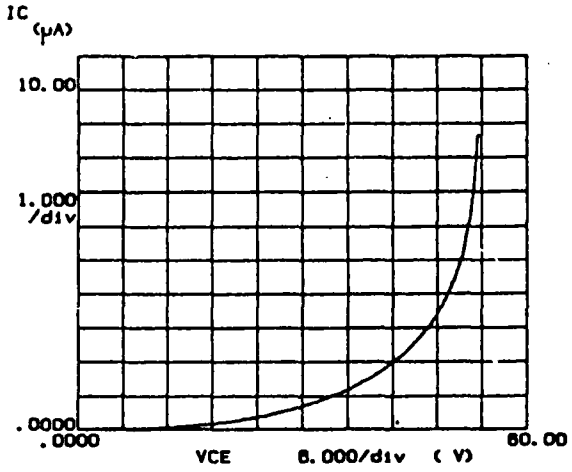
Variable1:
VCE -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 1.800mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



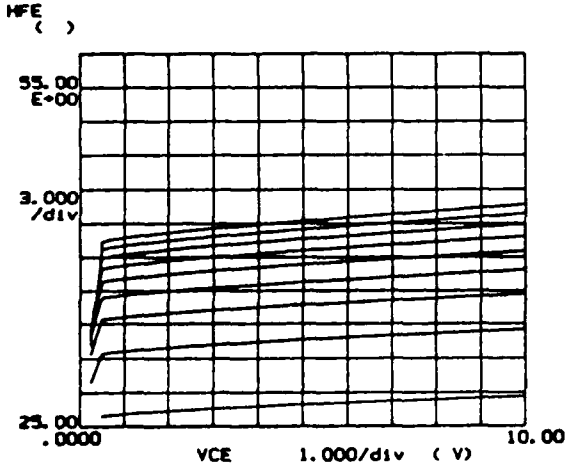
Variable1:
VCE -Ch1
Linear sweep
Start .0000V
Stop 80.000V
Step .8000V

Variable2:
IB -Ch2
Start .000 A
Step .000 A
Step .000 A

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



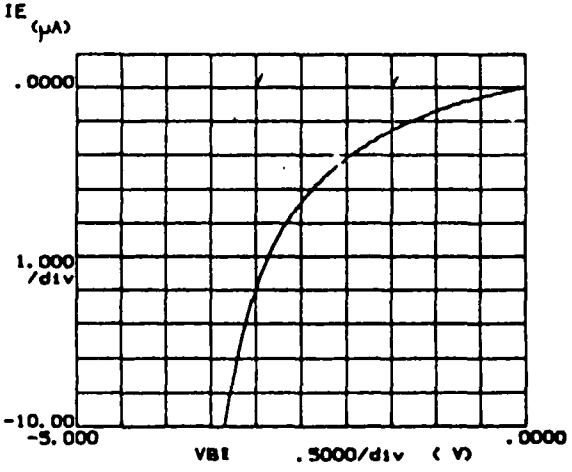
Variable1:
VCE -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 1.800mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

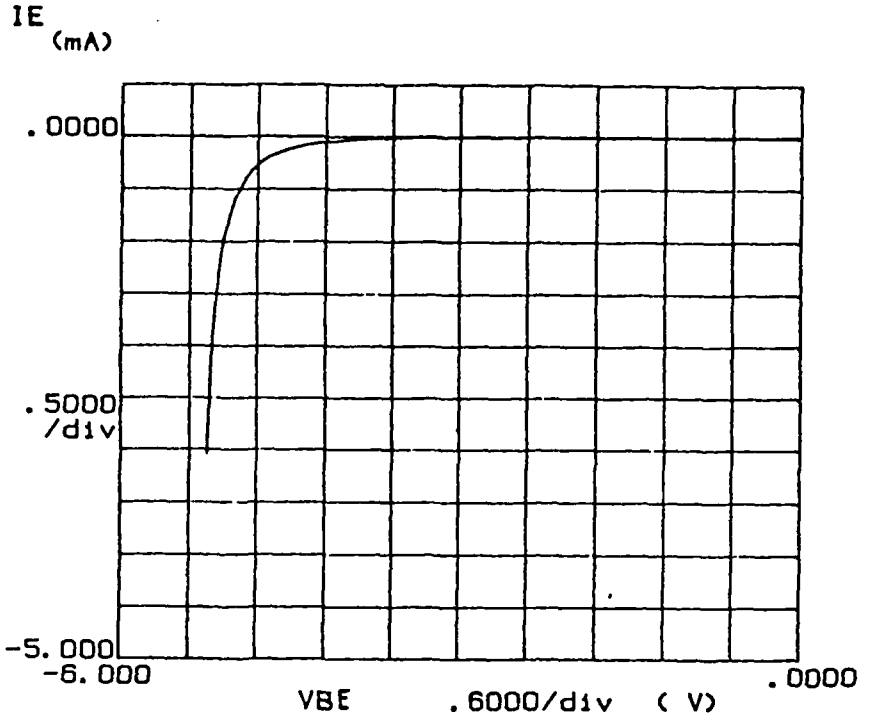
****** GRAPHICS PLOT ******



Variable1:
VE -Ch1
Linear sweep
Start .0000V
Step -5.0000V
Step -.0500V

Constants:
V -Ch2 .0000V

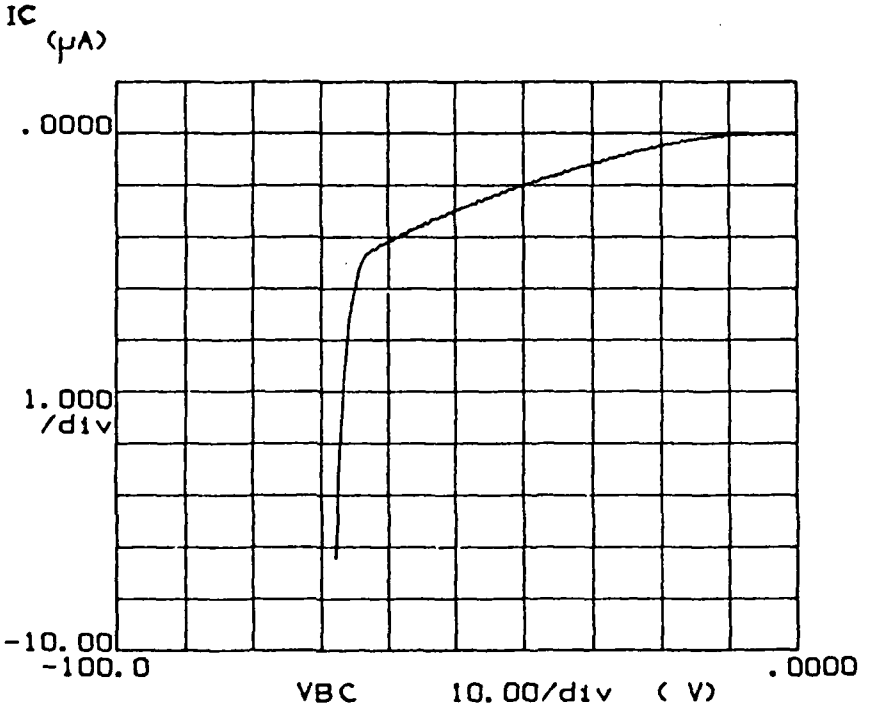
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -6.0000V
Step -.0500V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

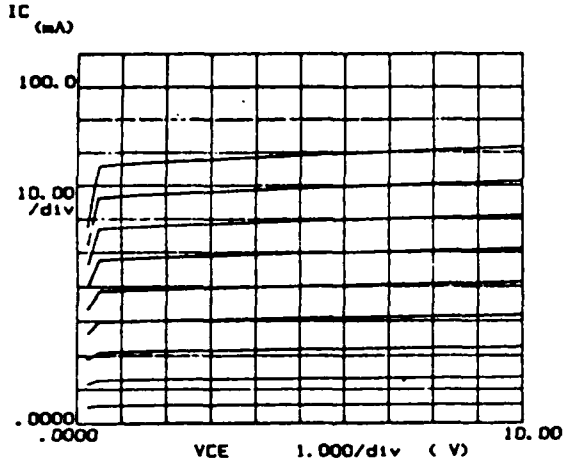


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -100.00V
Step -.5000V

Constants:
V -Ch3 .0000V

Figs. B.1.b

****** GRAPHICS PLOT ******



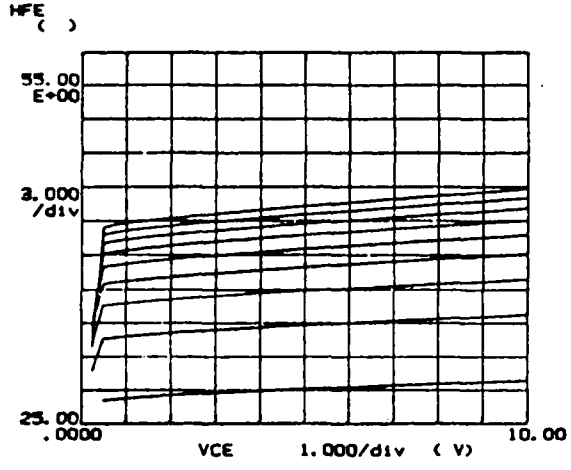
Variable1:
VCE -Ch1
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 1.800mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



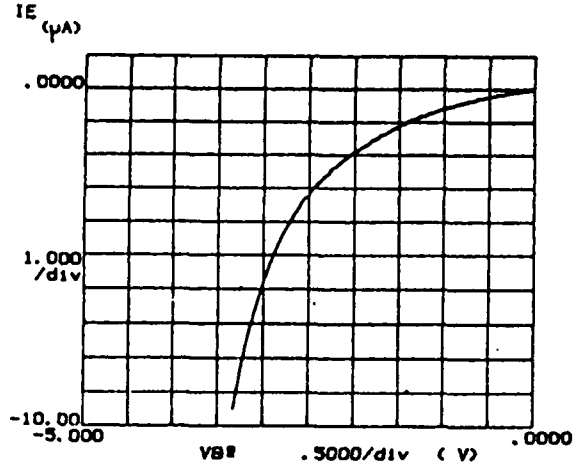
Variable1:
VCE -Ch1
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 1.800mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

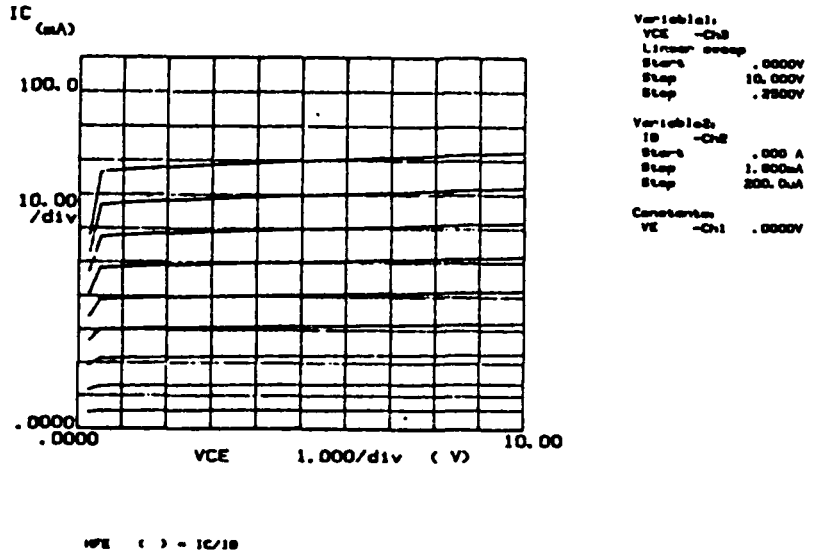
****** GRAPHICS PLOT ******

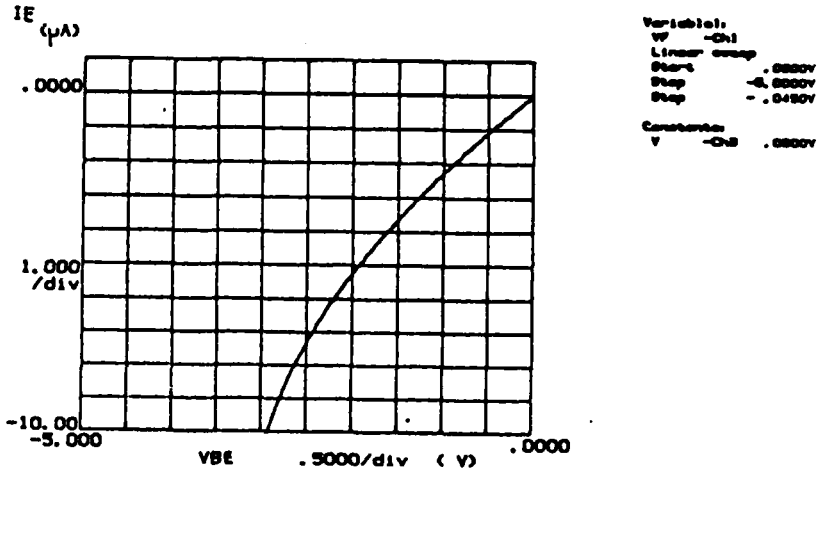


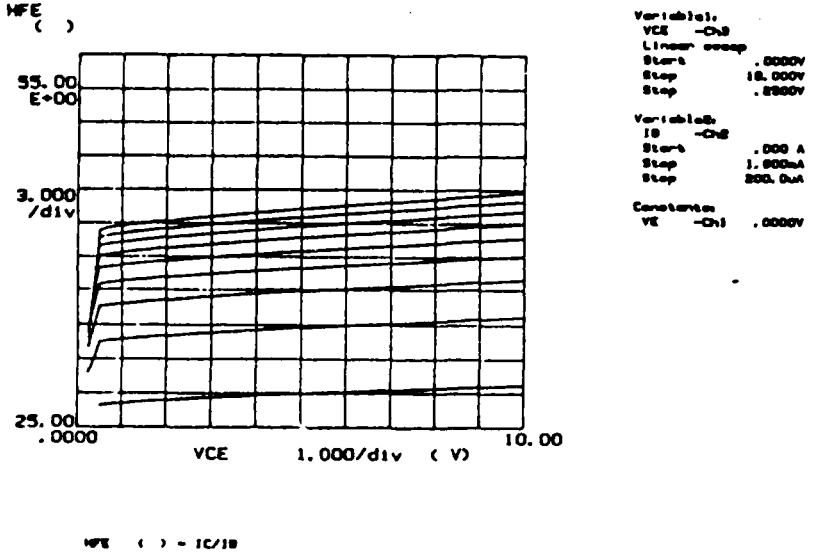
Variable1:
VE -Ch1
Linear sweep
Start .0000V
Step -5.0000V
Step -.0450V

Constants:
V -Ch2 .0000V

Figs. B.1.c

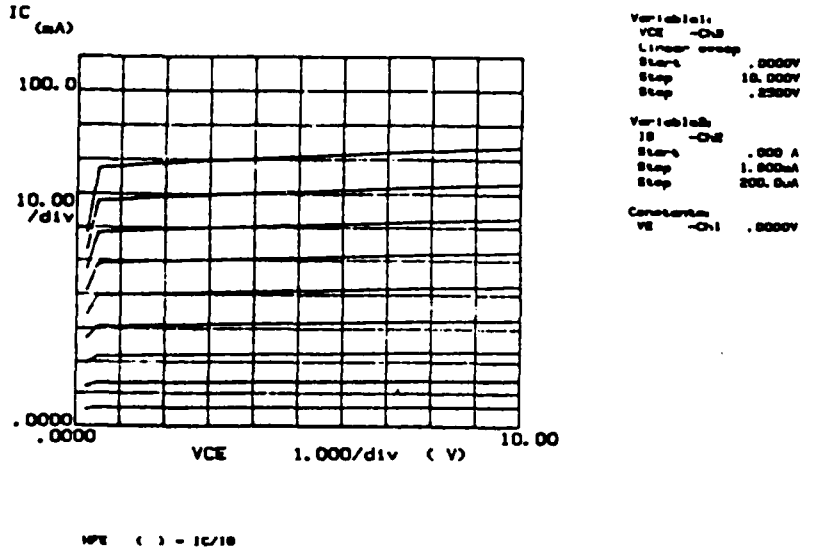

***** GRAPHICS PLOT *****
IC (mA)
100.0
10.00 /div
.0000
.0000
VCE 1.000/div (V)
10.00
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V
Variable2:
IB -Ch2
Start .000 A
Step 1.000mA
Step 200.0uA
Constants:
VE -Ch1 .0000V
HFE ( ) = IC/IB


***** GRAPHICS PLOT *****
IE (μA)
.0000
1.000 /div
-10.00
-5.000
VBE .5000/div (V)
.0000
Variable1:
W -Ch1
Linear sweep
Start .0000V
Step -5.0000V
Step -.5000V
Constants:
V -Ch3 .0000V


***** GRAPHICS PLOT *****
HFE ( )
55.00 E+00
3.000 /div
25.00
.0000
VCE 1.000/div (V)
10.00
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V
Variable2:
IB -Ch2
Start .000 A
Step 1.000mA
Step 200.0uA
Constants:
VE -Ch1 .0000V
HFE ( ) = IC/IB

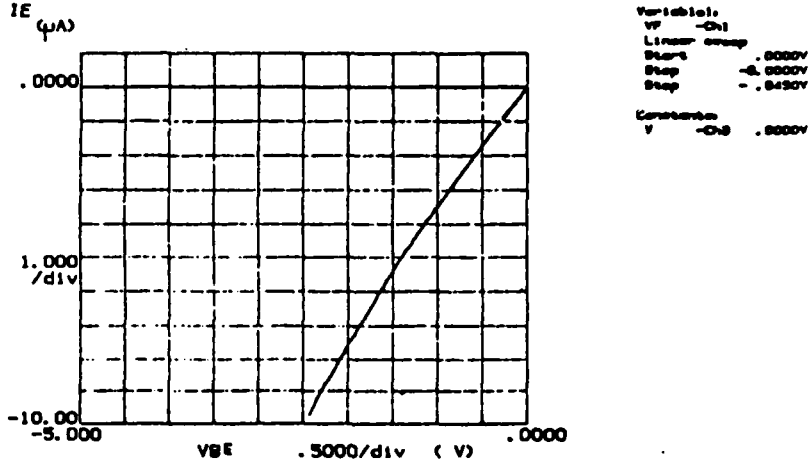
Figs. B.1.d

****** GRAPHICS PLOT ******

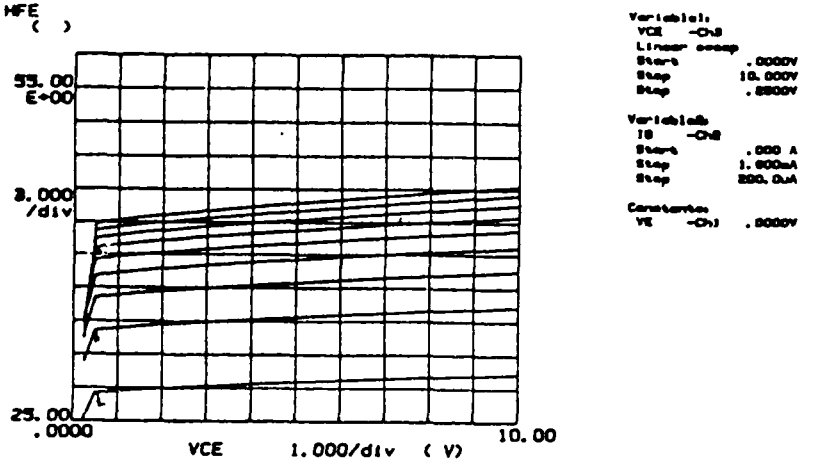


HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



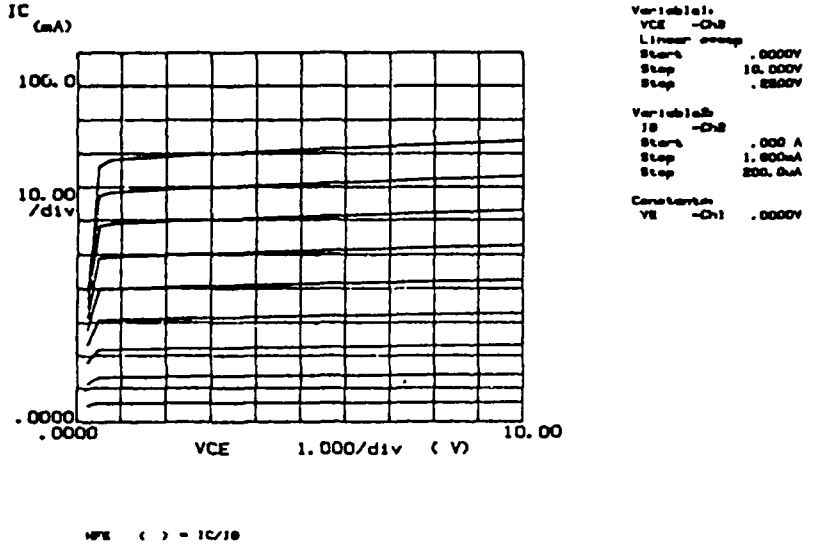
****** GRAPHICS PLOT ******



HFE ( ) = IC/IB

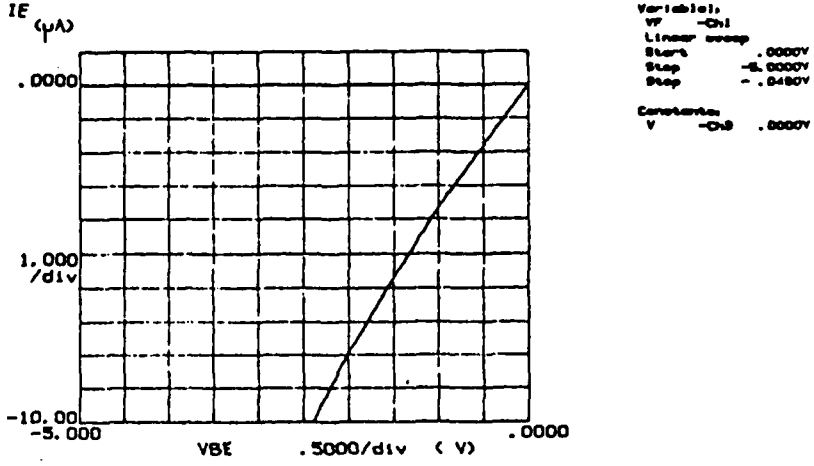
Figs. B.1.e

****** GRAPHICS PLOT ******

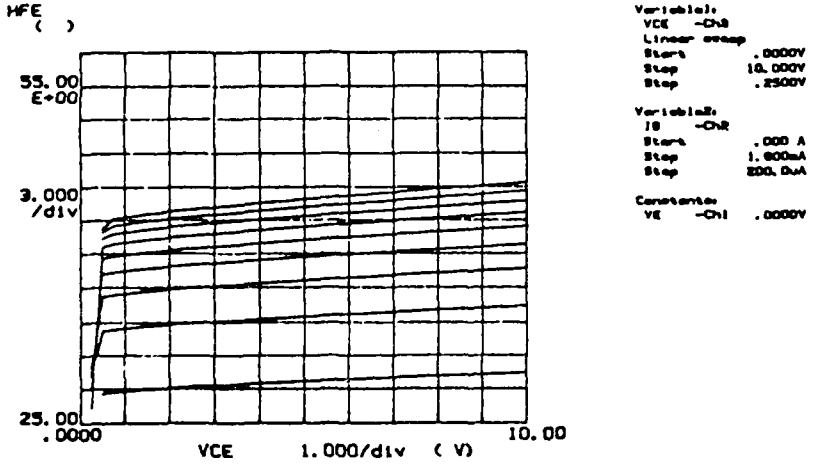


HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



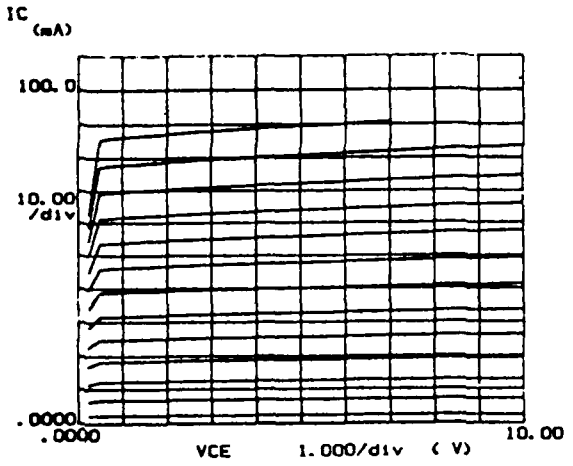
****** GRAPHICS PLOT ******



HFE ( ) = IC/IB

Figs. B.1.f

****** GRAPHICS PLOT ******



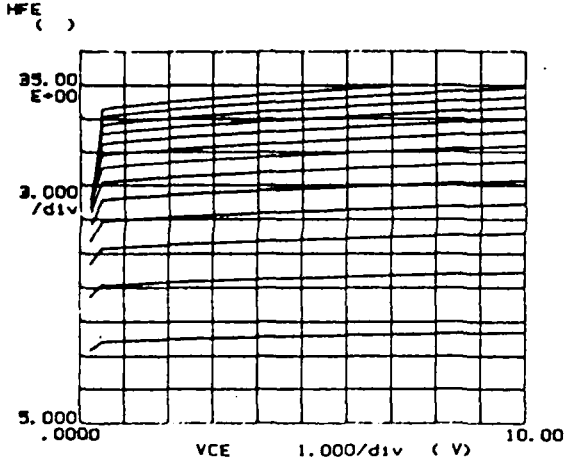
Variable1:
VCE -Ch1
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.000mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



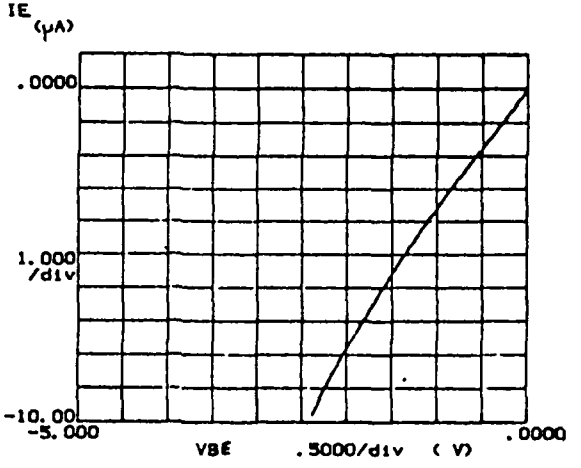
Variable1:
VCE -Ch1
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.000mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

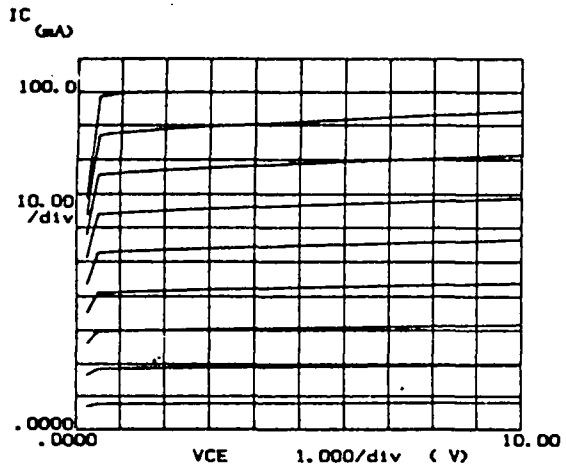


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -5.0000V
Step -.0490V

Constants:
V -Ch2 .0000V

Figs. B.2.a

****** GRAPHICS PLOT ******



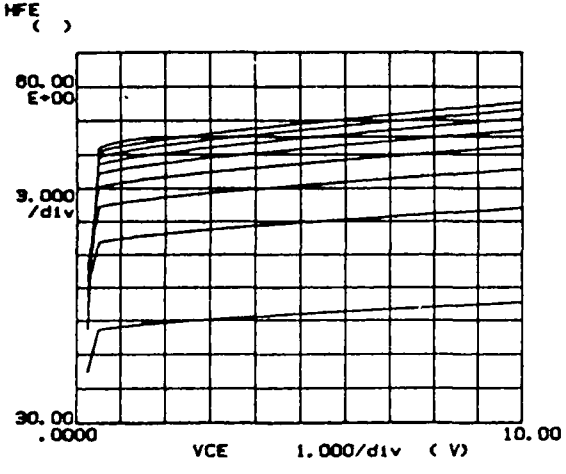
Variable1:
VCE -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 1.800mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



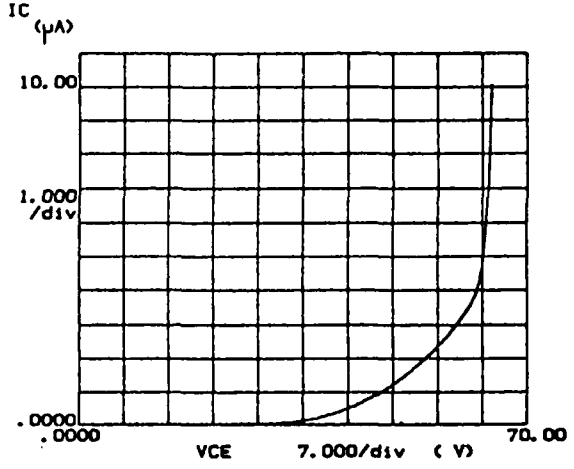
Variable1:
VCE -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 1.800mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



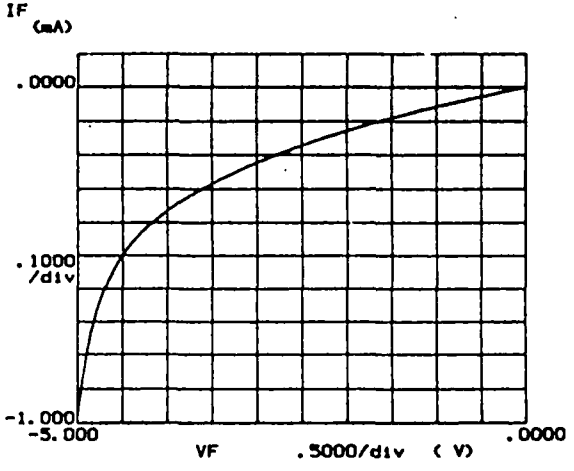
Variable1:
VCE -Ch1
Linear sweep
Start .0000V
Stop 70.000V
Step .5000V

Variable2:
IB -Ch2
Start .000 A
Step .000 A
Step .000 A

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

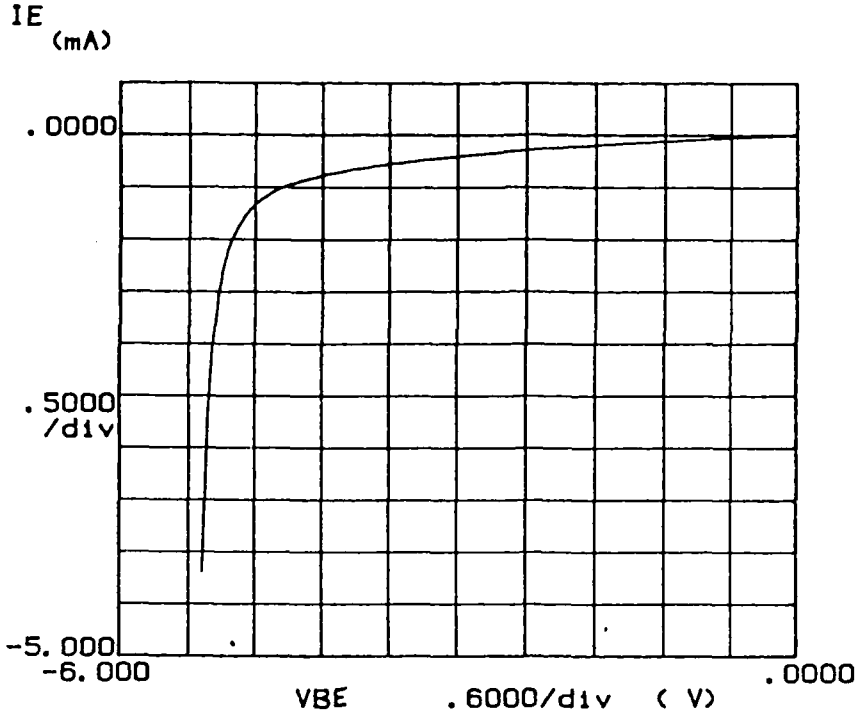
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -5.0000V
Step -.0500V

Constants:
V -Ch2 .0000V

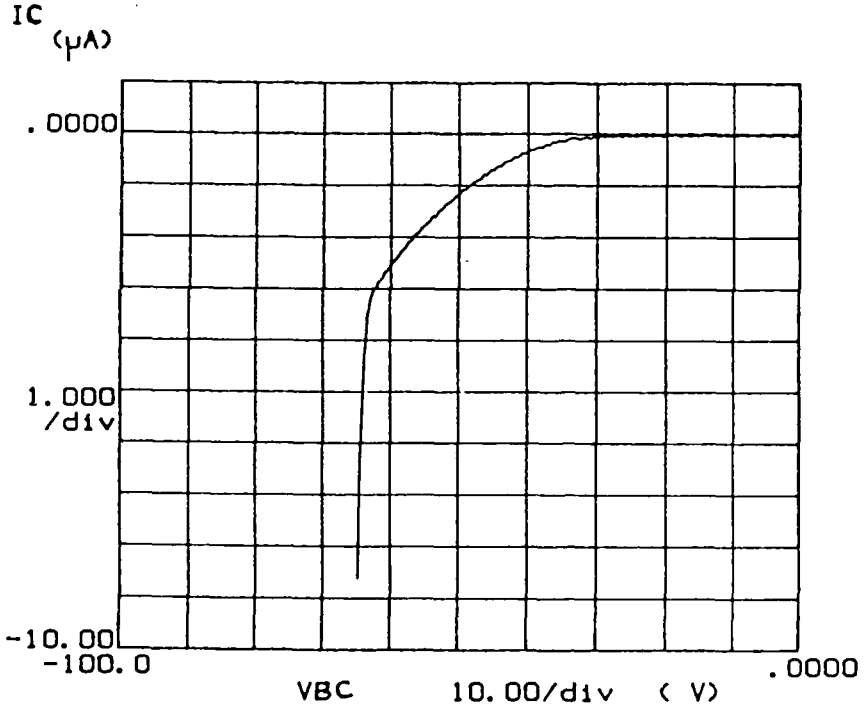
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -6.0000V
Step -.0480V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

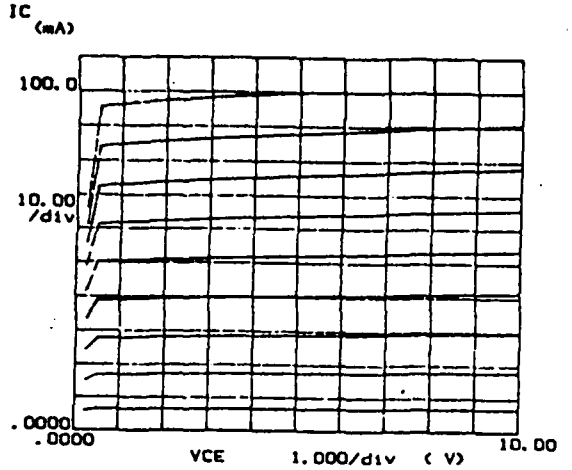


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -100.00V
Step -.5000V

Constants:
V -Ch3 .0000V

Figs. B.2.b

****** GRAPHICS PLOT ******



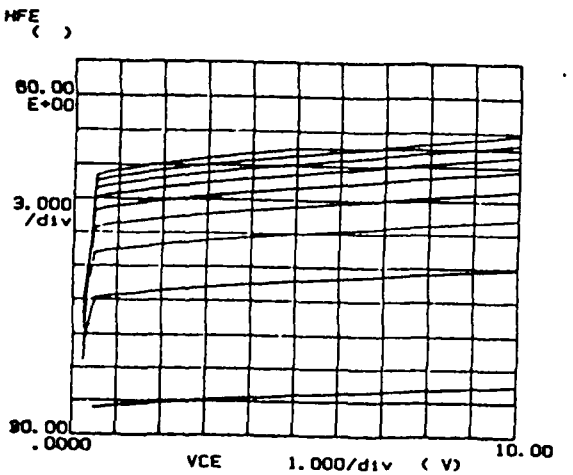
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 1.800mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



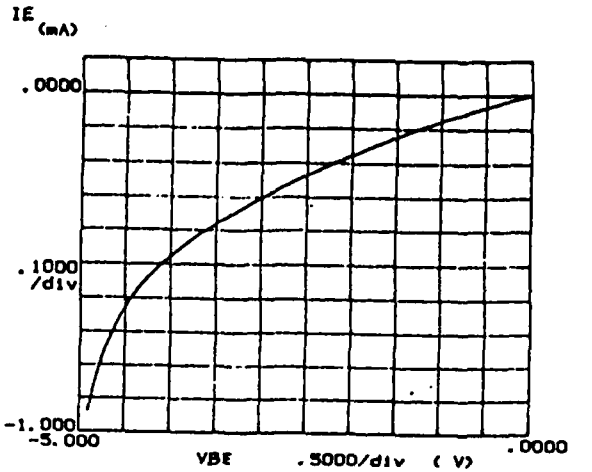
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 1.800mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

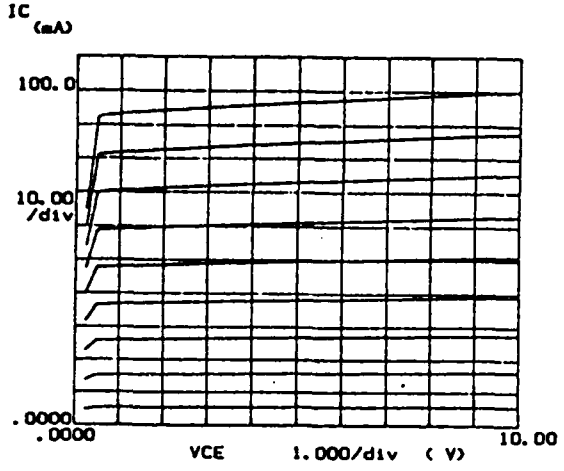


Variable1:
VBE -Ch1
Linear sweep
Start .0000V
Step -5.0000V
Step -.0500V

Constants:
VCE -Ch2 .0000V

Figs. B.2.c

****** GRAPHICS PLOT ******



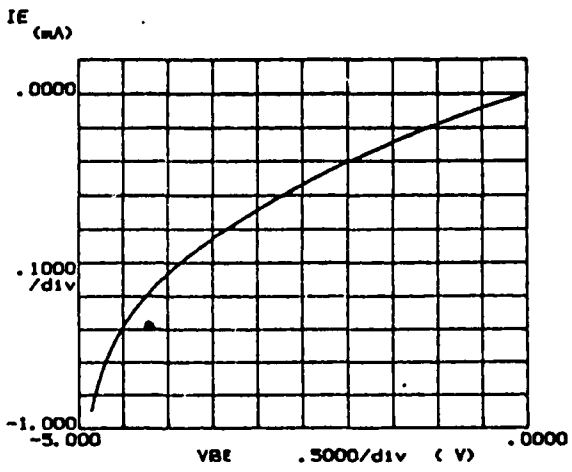
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch1
Start .000 A
Step 1.800mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

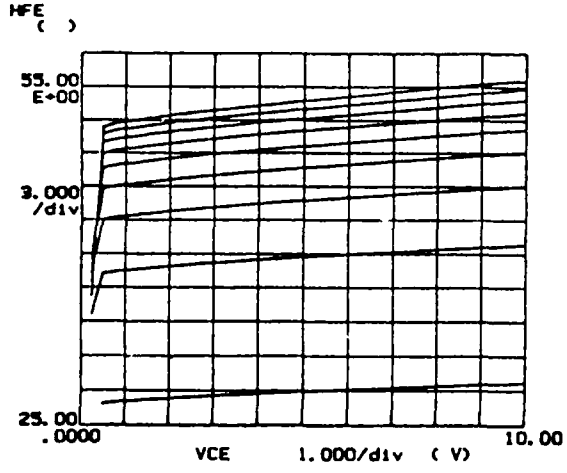
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -5.0000V
Step -.8438V

Constants:
V -Ch2 .0000V

****** GRAPHICS PLOT ******



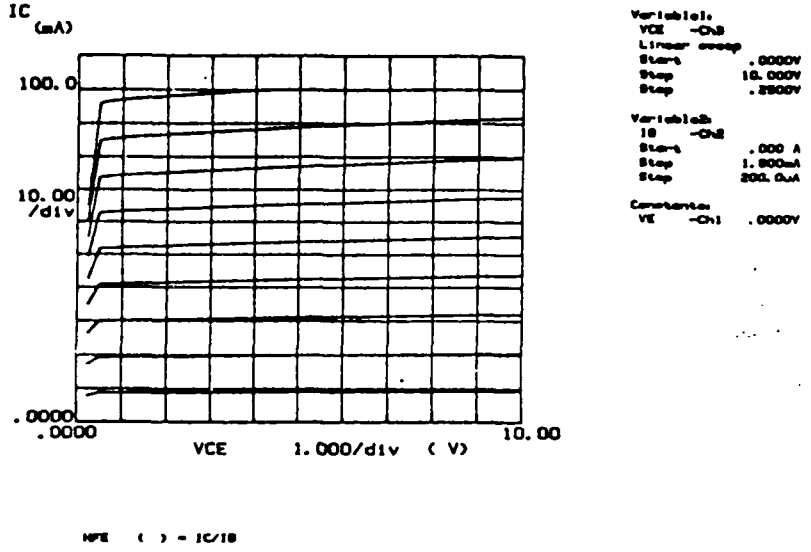
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch1
Start .000 A
Step 1.800mA
Step 200.0uA

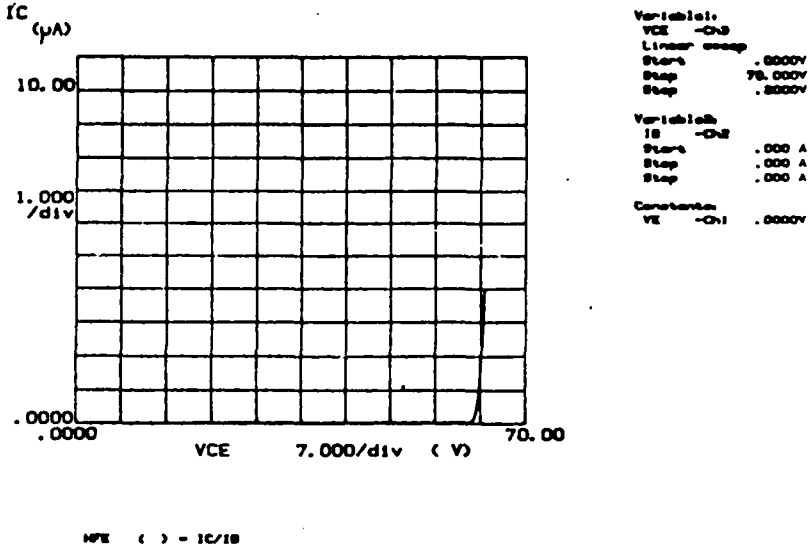
Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

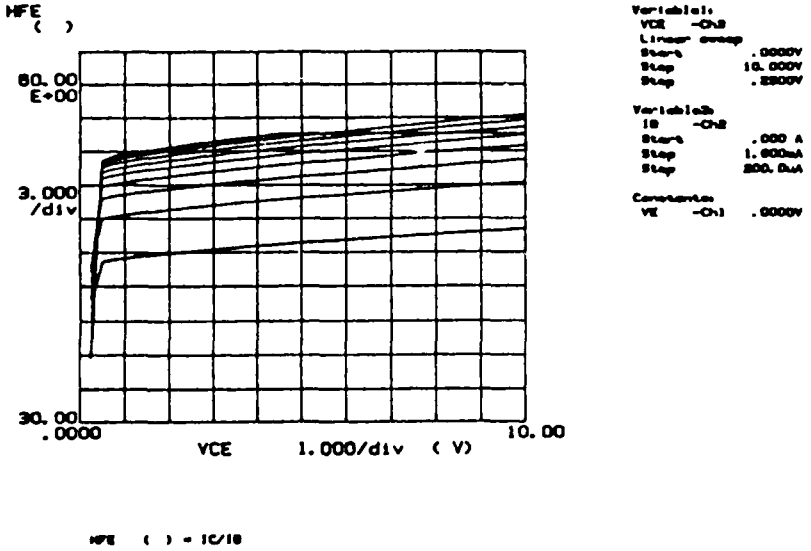
****** GRAPHICS PLOT ******



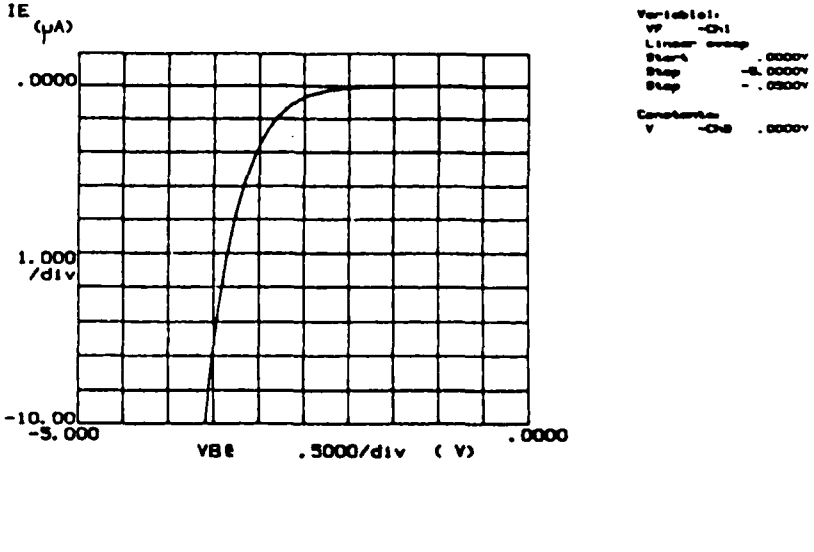
****** GRAPHICS PLOT ******



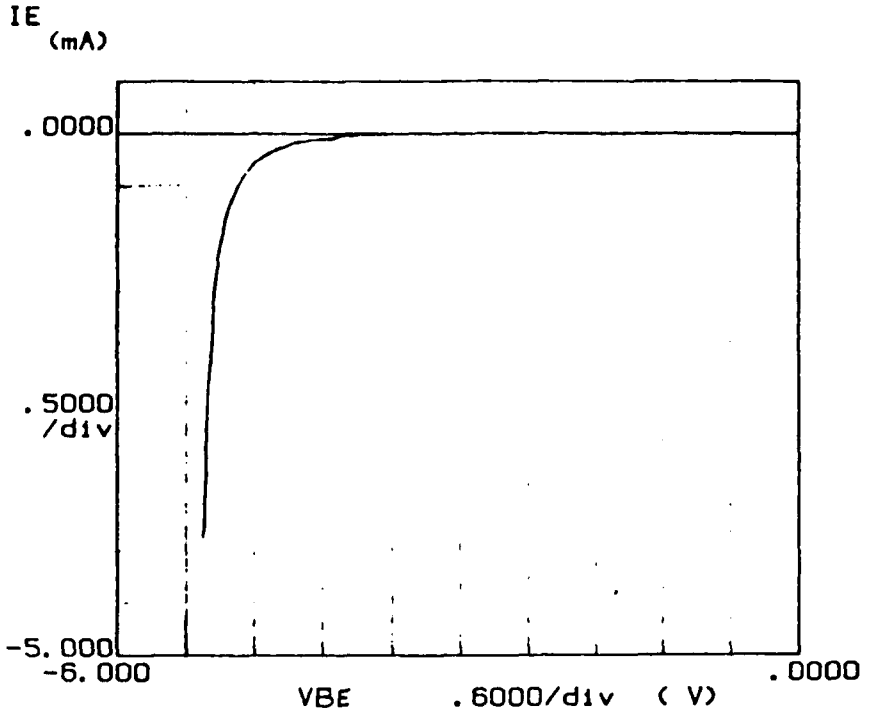
****** GRAPHICS PLOT ******



****** GRAPHICS PLOT ******

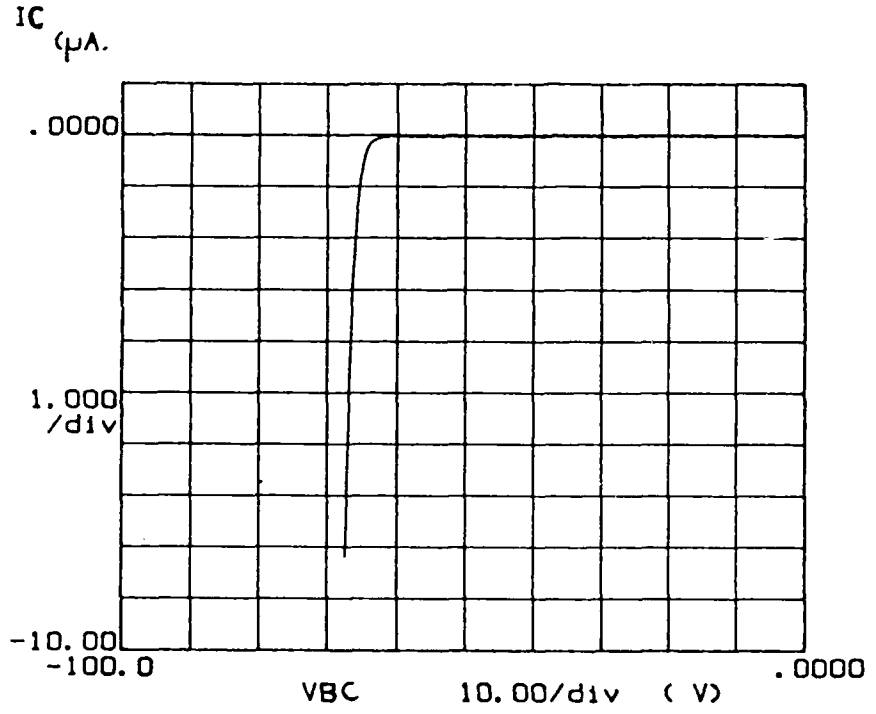


****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -6.0000V
Step - .0500V

Constants:
V -Ch3 .0000V

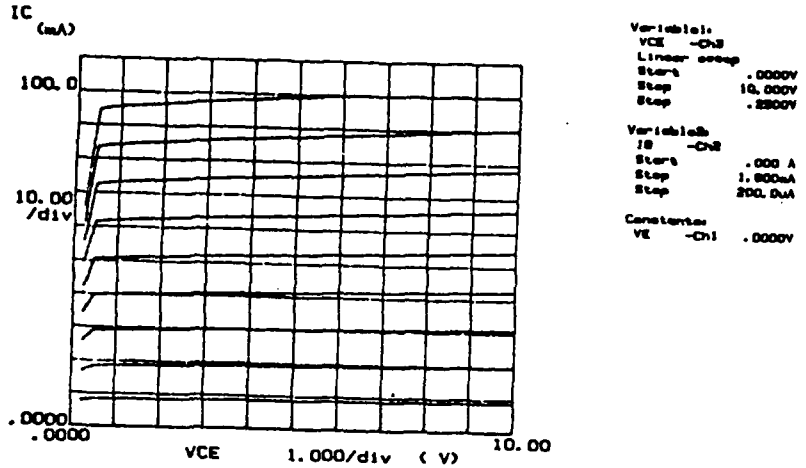


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -100.00V
Step - .5000V

Constants:
V -Ch3 .0000V

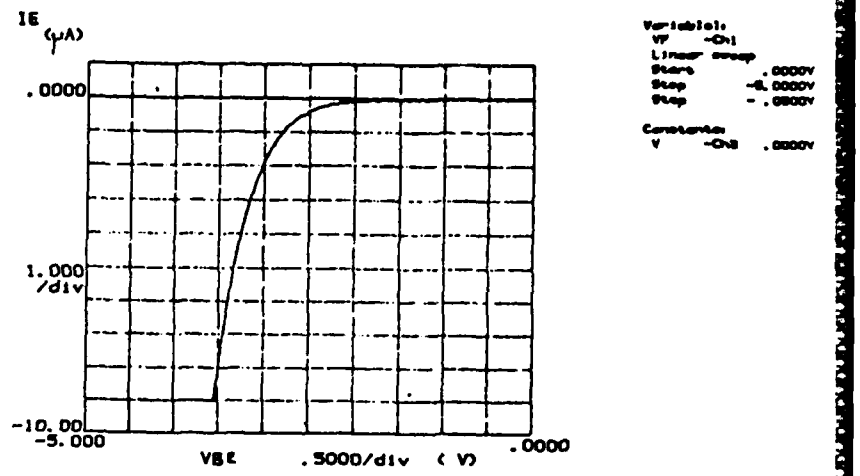
Figs. B.3.d

****** GRAPHICS PLOT ******

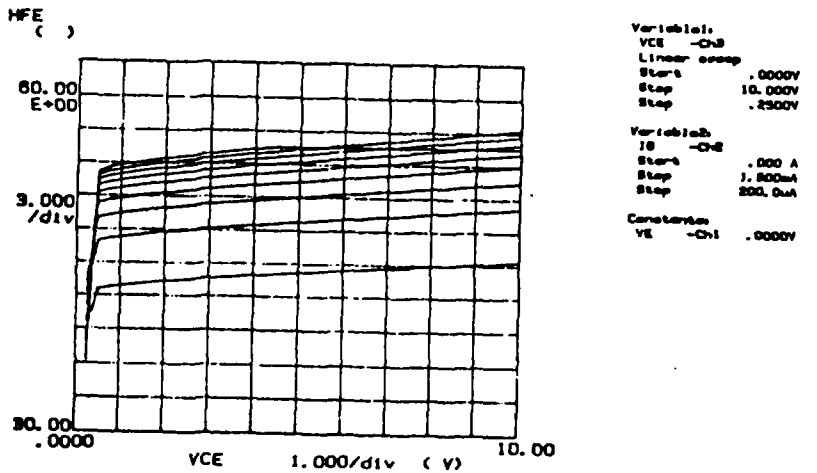


HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



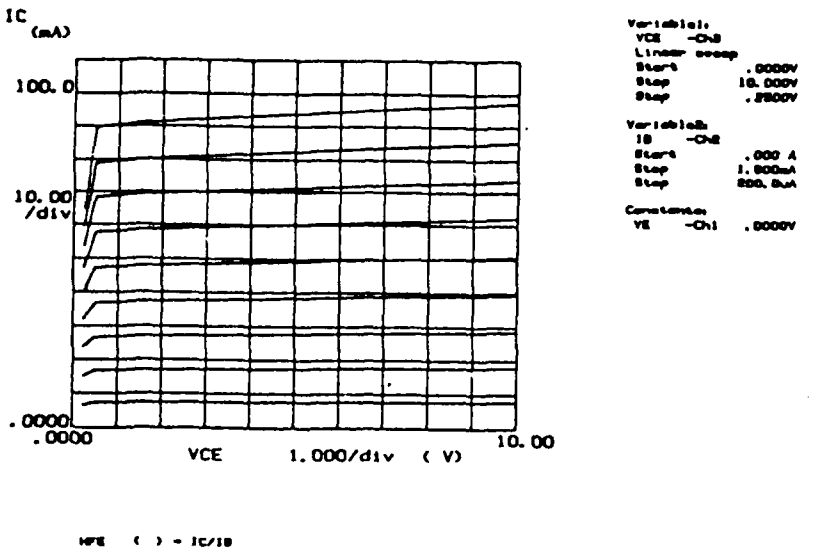
****** GRAPHICS PLOT ******



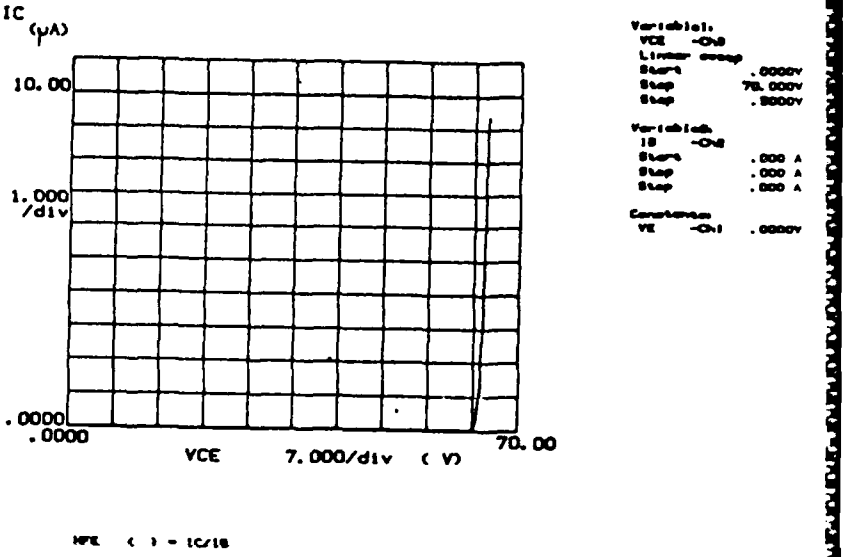
HFE ( ) = IC/IB

Figs. B.4.a

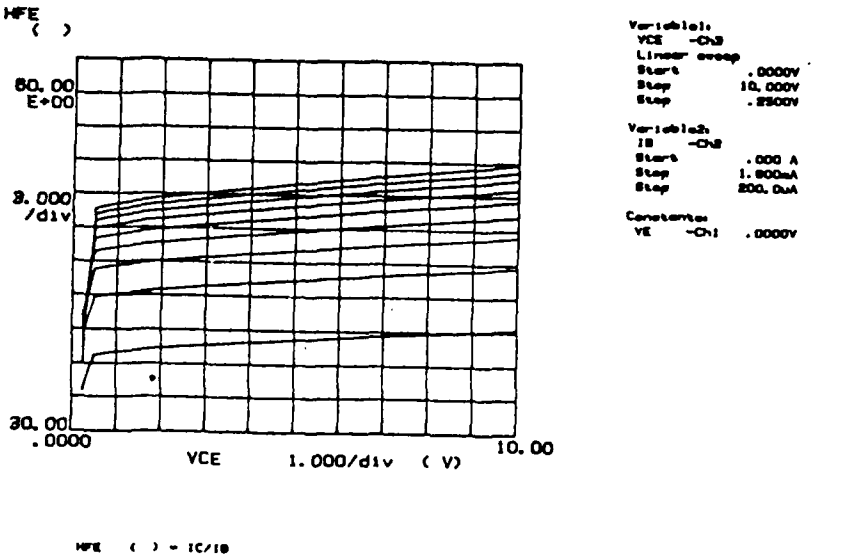
****** GRAPHICS PLOT ******



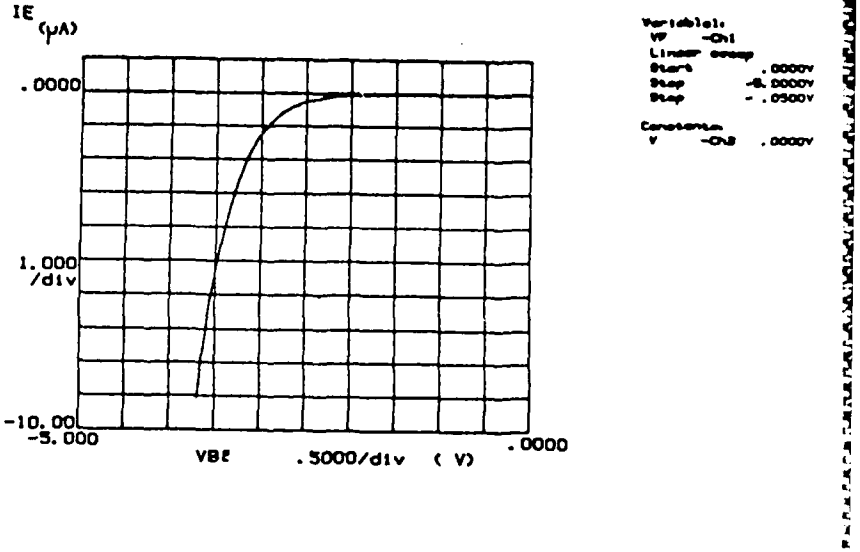
****** GRAPHICS PLOT ******



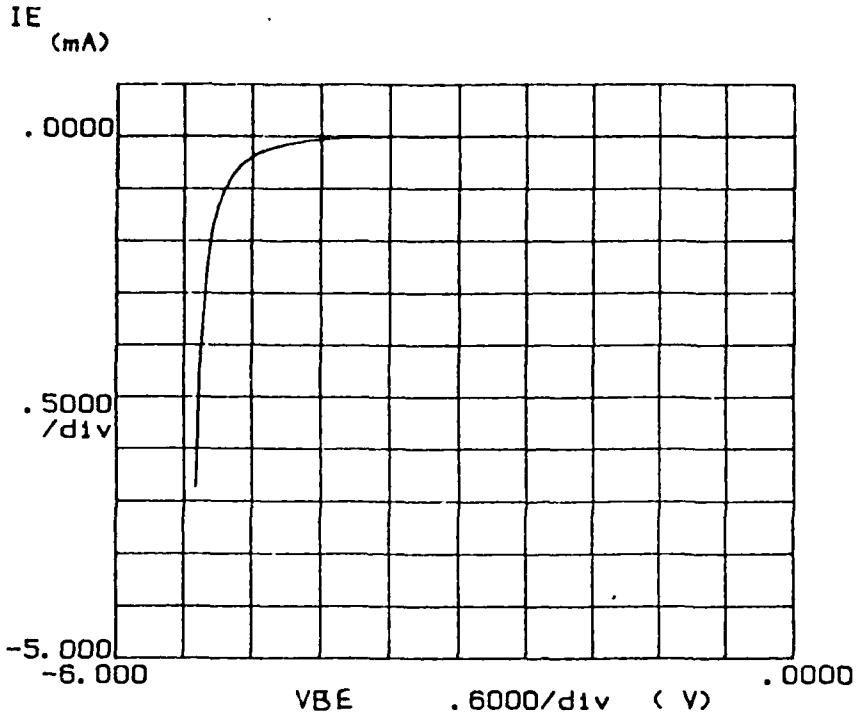
****** GRAPHICS PLOT ******



****** GRAPHICS PLOT ******



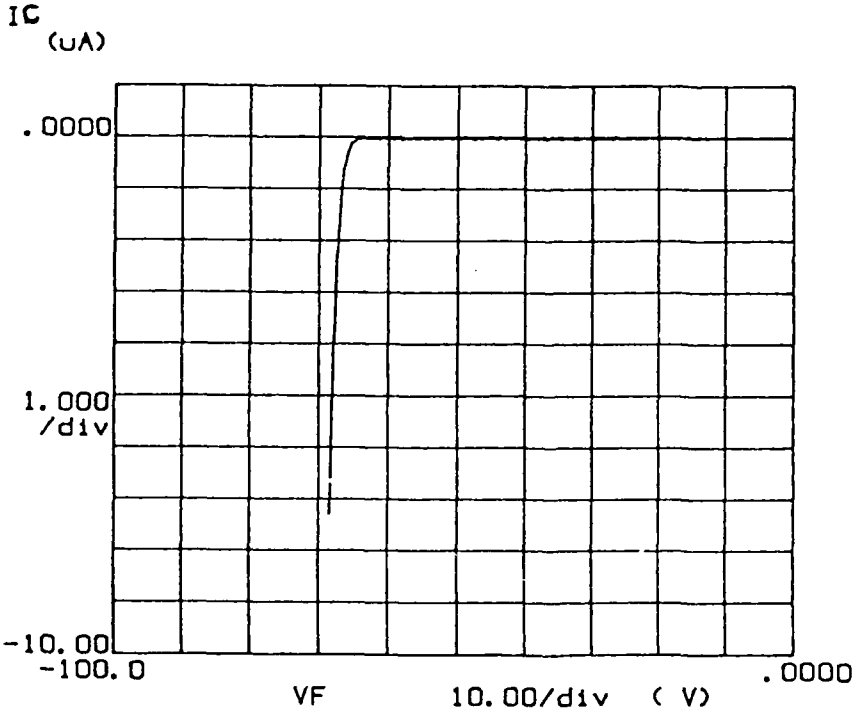
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -6.0000V
Step -.0500V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******

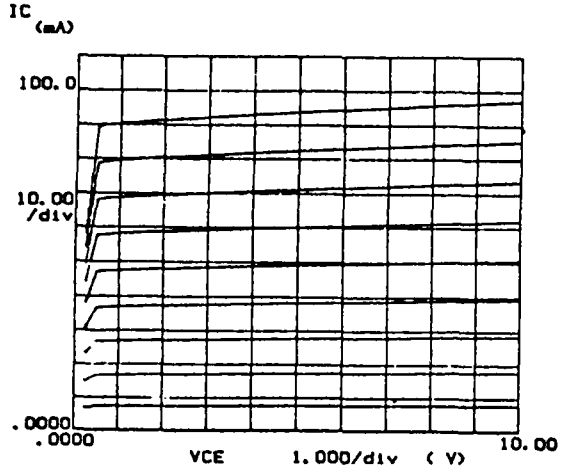


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -100.00V
Step -.5000V

Constants:
V -Ch3 .0000V

Figs. B.4.e

****** GRAPHICS PLOT ******



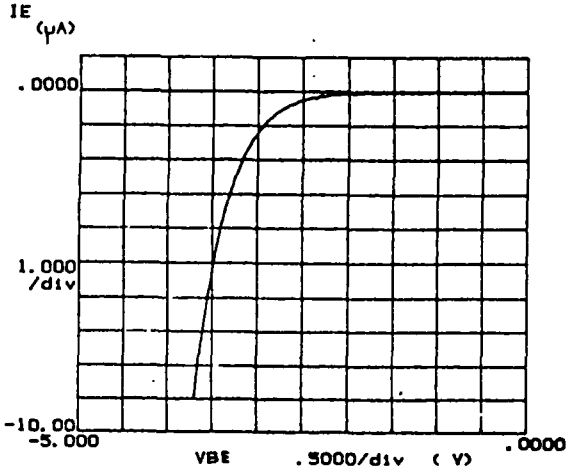
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 1.800mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

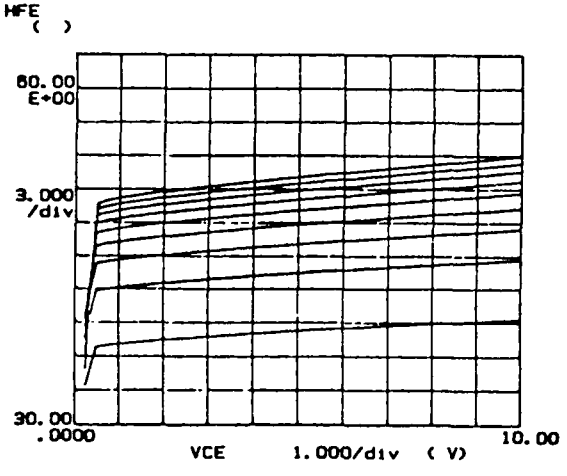
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -5.0000V
Step -.0500V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******



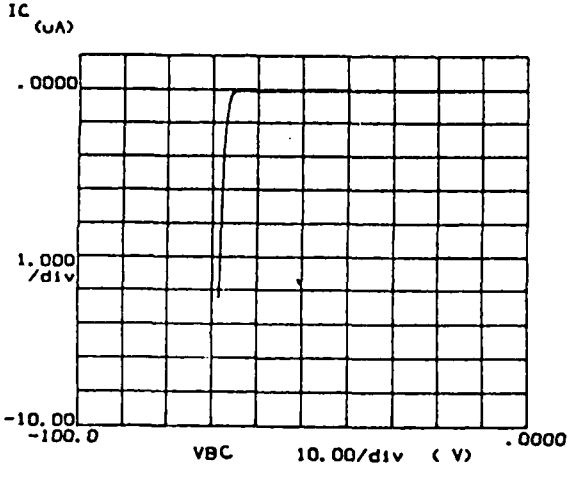
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 1.800mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

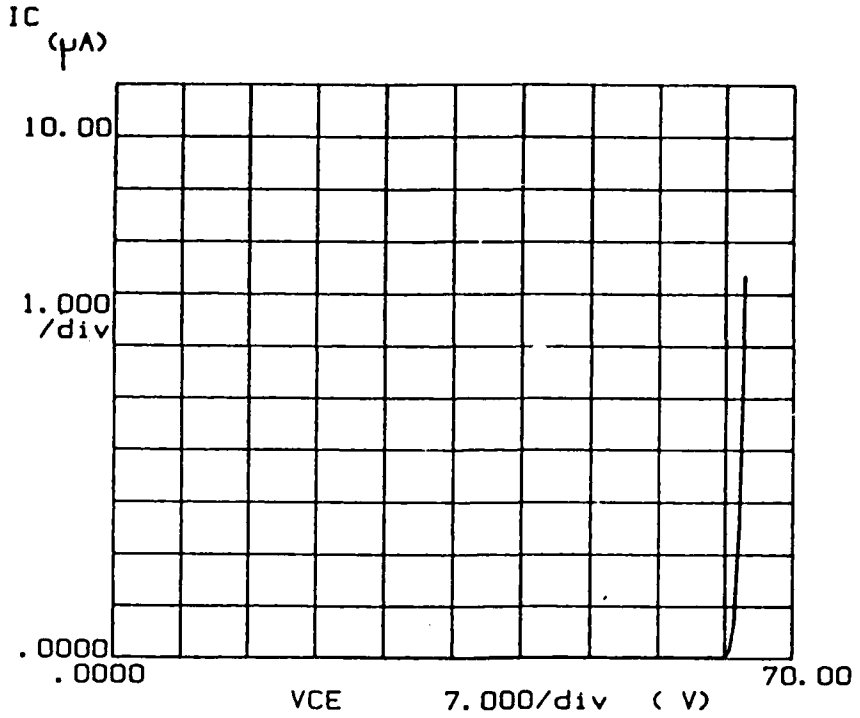
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -100.00V
Step -.5000V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******



Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 70.000V
Step .5000V

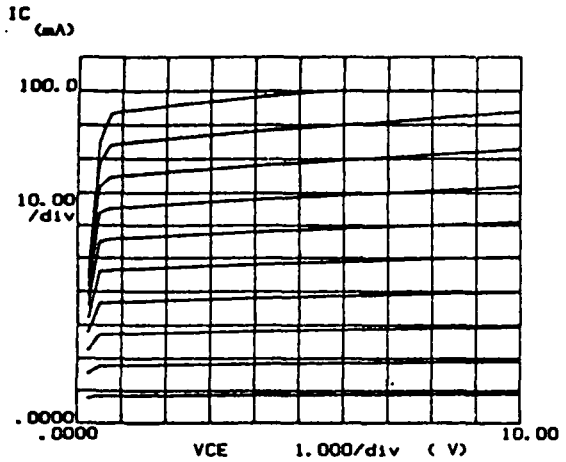
Variable2:
IB -Ch2
Start .000 A
Stop .000 A
Step .000 A

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

Figs. C.1.a

****** GRAPHICS PLOT ******



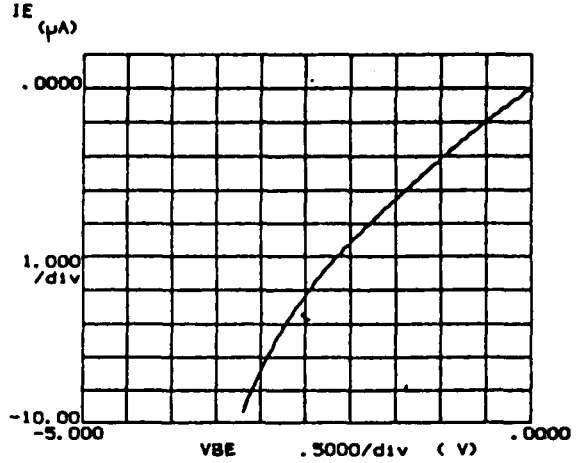
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.000mA
Step 200.0uA

Constant:
VE -Ch1 .0000V

HFE ( ) = IC/IB

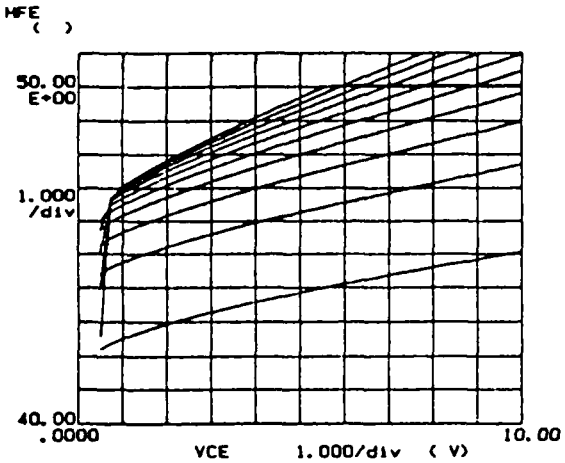
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -5.0000V
Step -.0430V

Constant:
V -Ch2 .0000V

****** GRAPHICS PLOT ******



Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Step 10.000V
Step .2500V

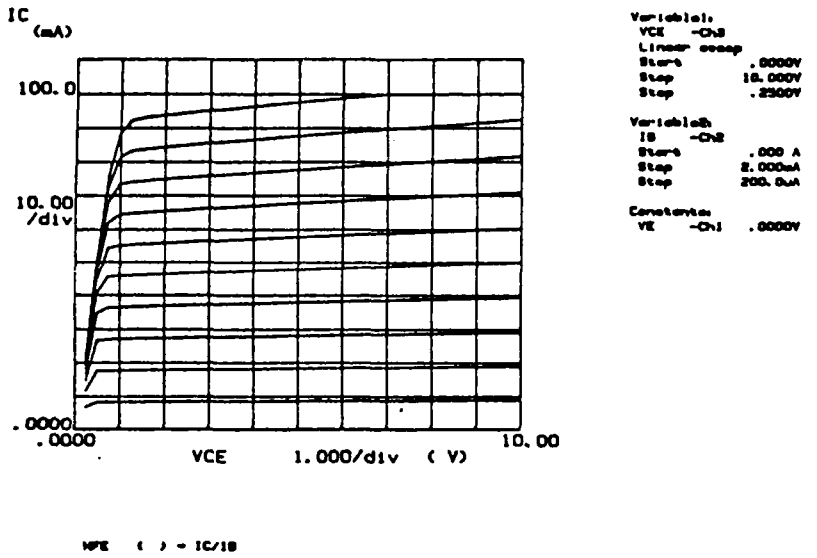
Variable2:
IB -Ch2
Start .000 A
Step 2.000mA
Step 200.0uA

Constant:
VE -Ch1 .0000V

HFE ( ) = IC/IB

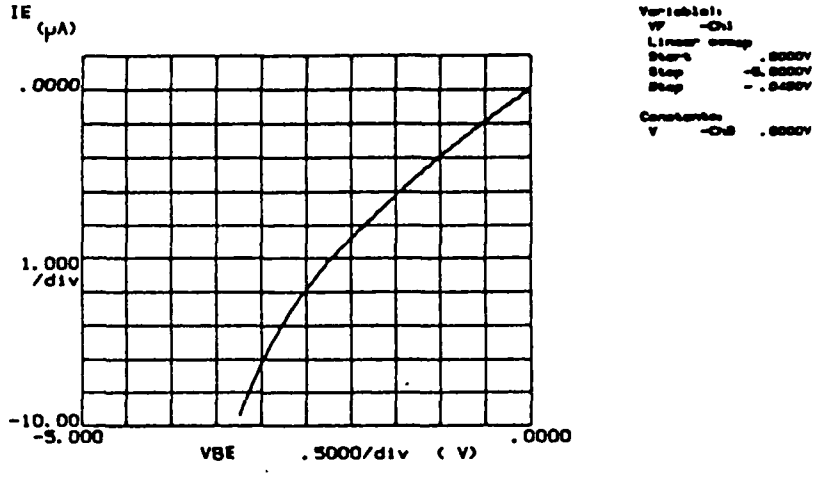
Figs. C.1.c

****** GRAPHICS PLOT ******

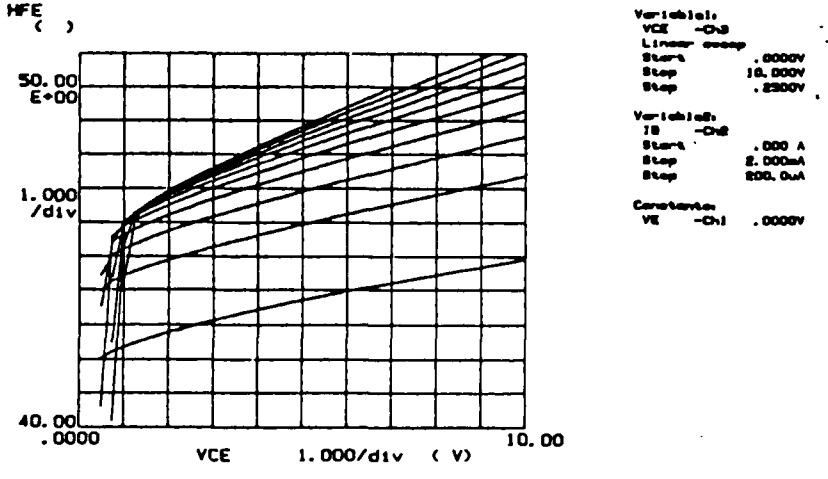


HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



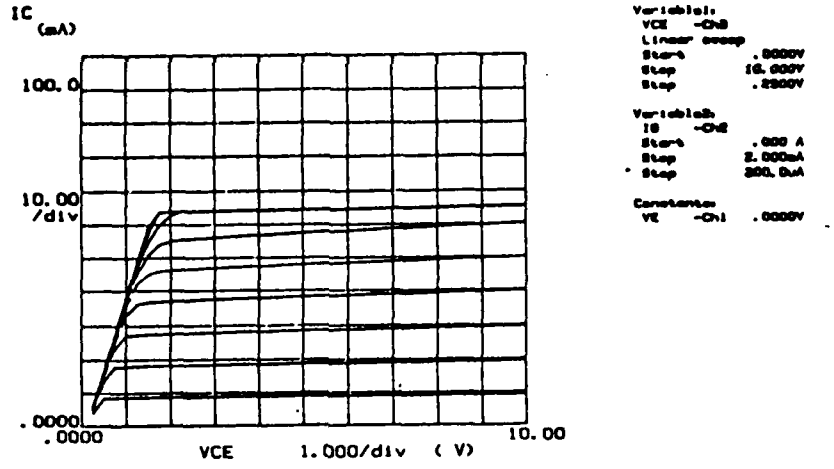
****** GRAPHICS PLOT ******



HFE ( ) = IC/IB

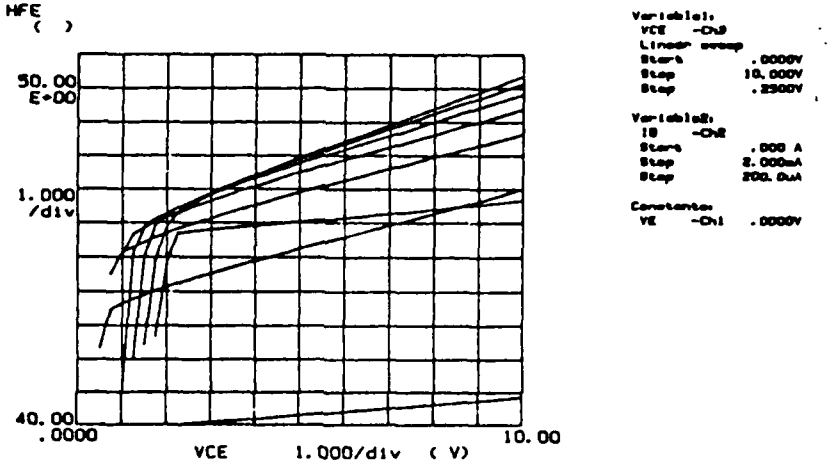
Figs. C.1.d

****** GRAPHICS PLOT ******



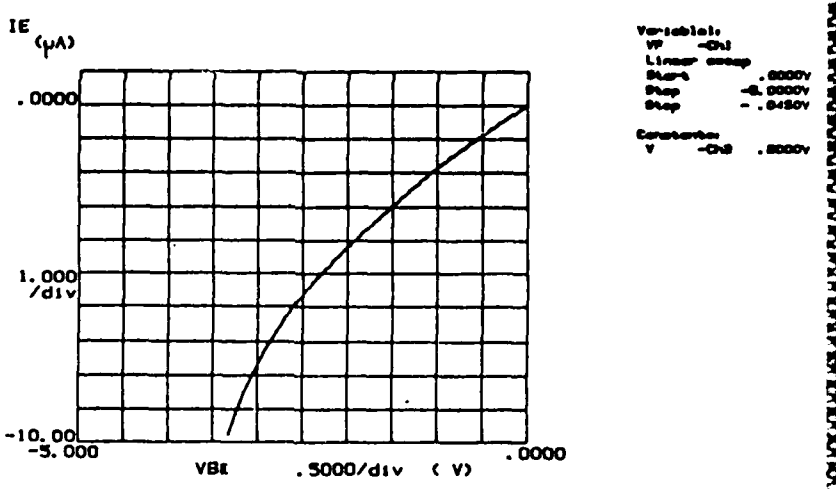
HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

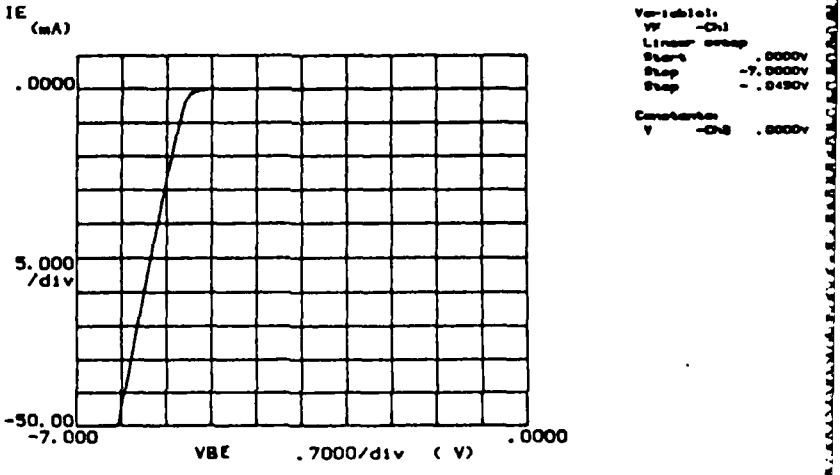


HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

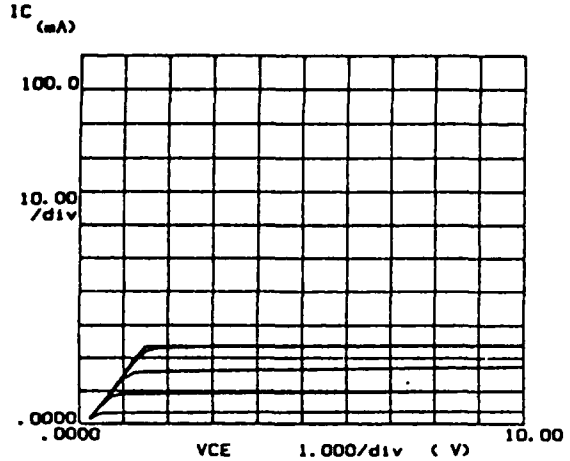


****** GRAPHICS PLOT ******



Figs. C.1.e

****** GRAPHICS PLOT ******



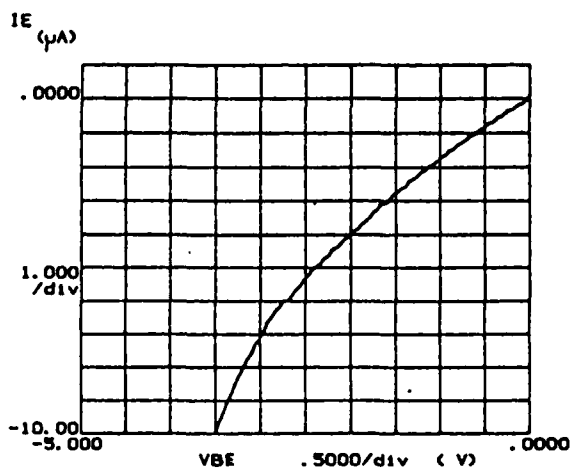
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch1
Start .000 A
Stop 2.000mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

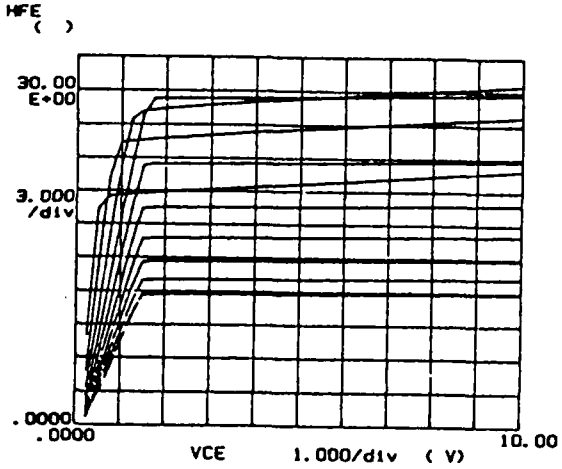
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -5.0000V
Step -.0450V

Constants:
V -Ch2 .0000V

****** GRAPHICS PLOT ******



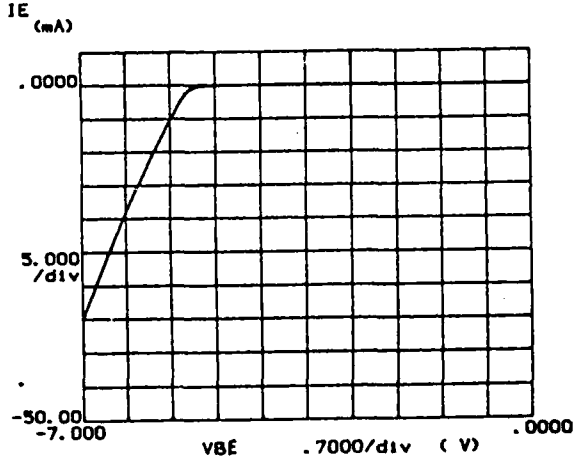
Variable1:
VCE -Ch2
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch1
Start .000 A
Stop 2.000mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

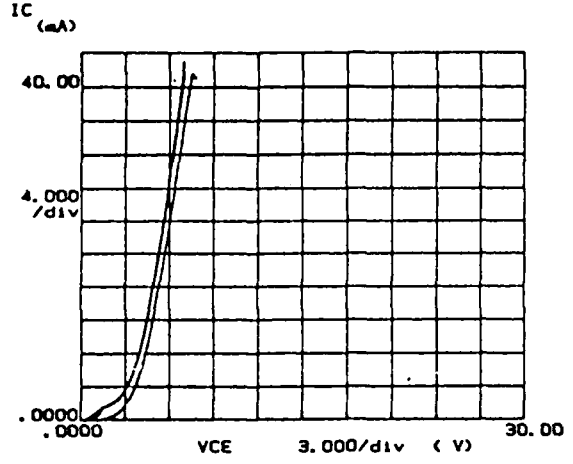


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -7.0000V
Step -.0450V

Constants:
V -Ch2 .0000V

Figs. C.1.f

****** GRAPHICS PLOT ******



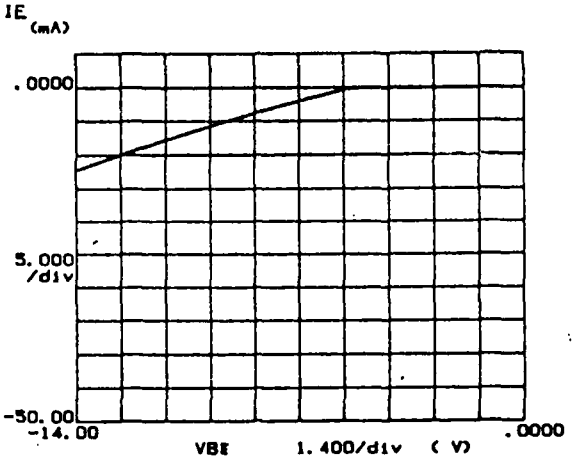
Variable1:
VCE -Ch8
Linear sweep
Start .0000V
Stop 30.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.000mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

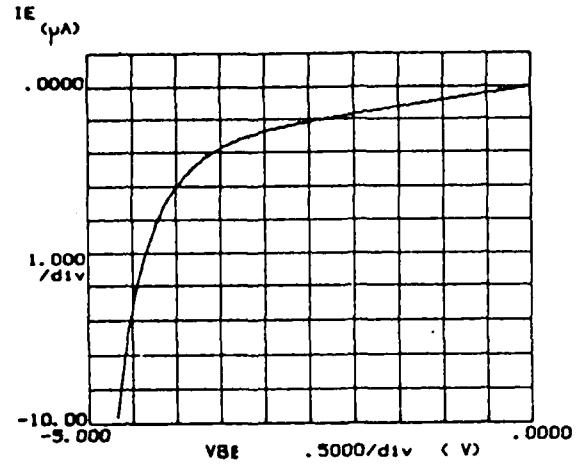
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -14.000V
Step -.0480V

Constants:
V -Ch8 .0000V

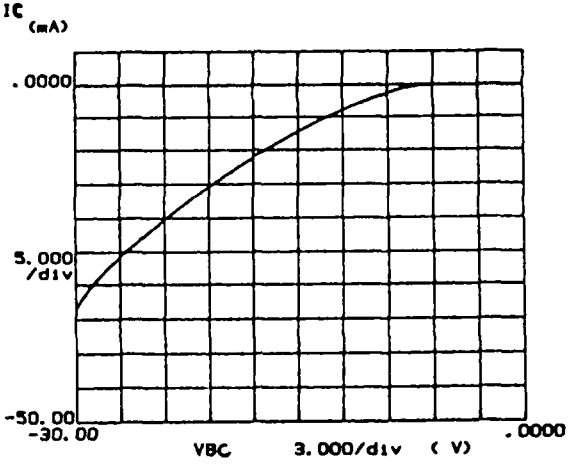
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -8.0000V
Step -.0480V

Constants:
V -Ch8 .0000V

****** GRAPHICS PLOT ******

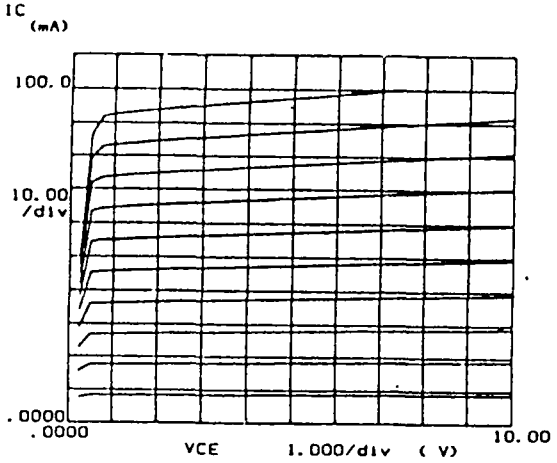


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Step -30.000V
Step -.2000V

Constants:
V -Ch8 .0000V

Figs. C.2.a

****** GRAPHICS PLOT ******



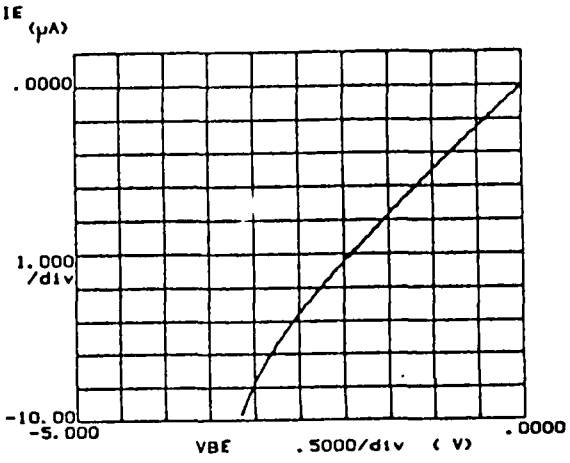
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Step 2.000mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

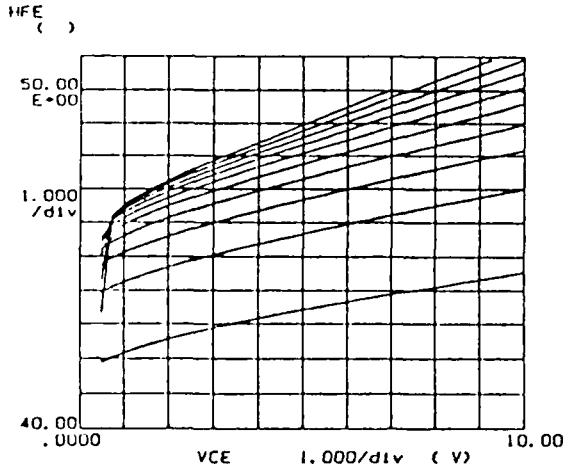
****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -5.0000V
Step -.0450V

Constants:
V -Ch3 .0000V

****** GRAPHICS PLOT ******



Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

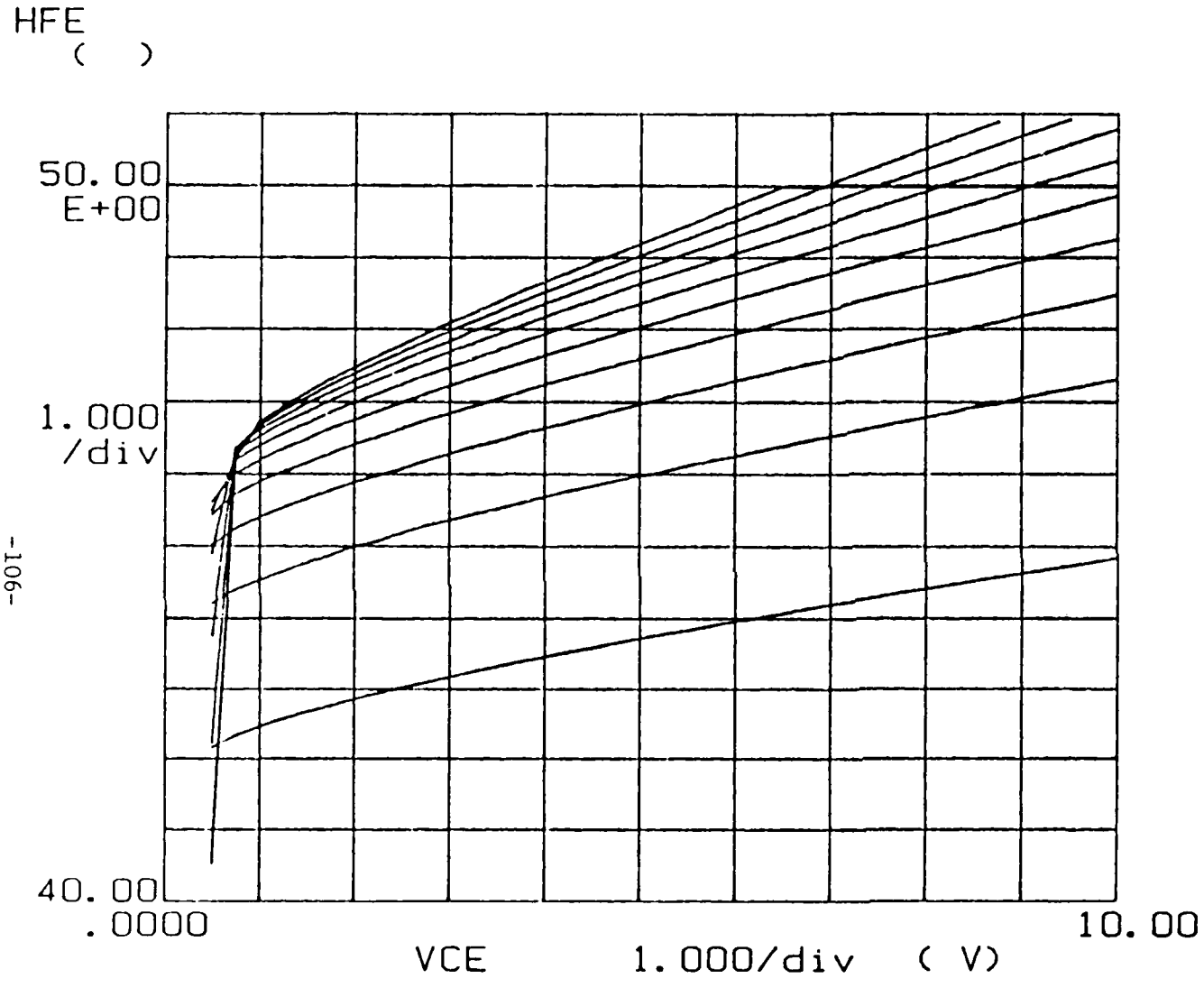
Variable2:
IB -Ch2
Start .000 A
Step 2.000mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

Figs. C.2.b

****** GRAPHICS PLOT ******



Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

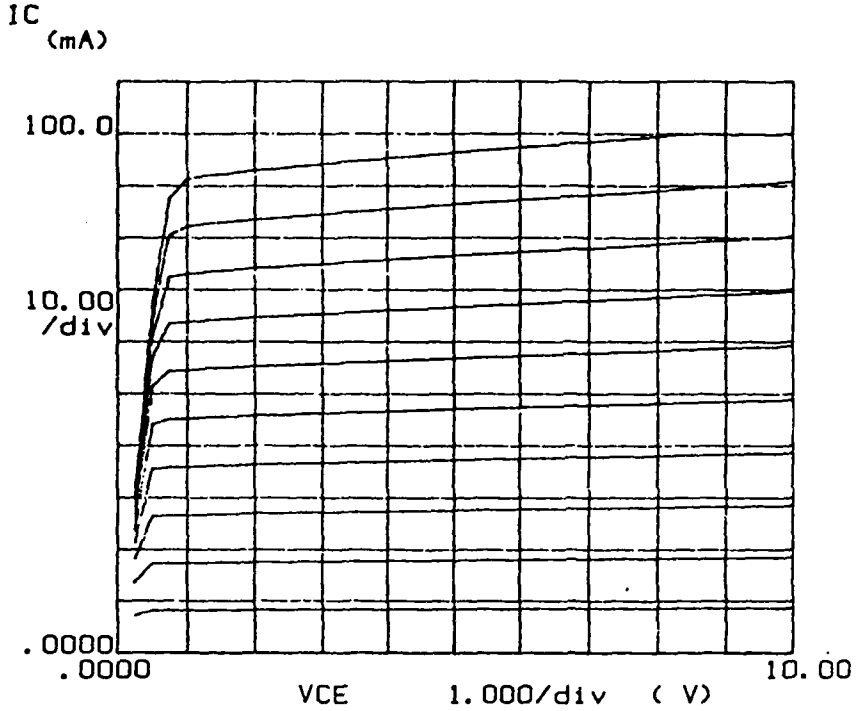
Variable2:
IB -Ch2
Start .000 A
Stop 2.000mA
Step 200.0uA

Constante:
VE -Ch1 .0000V

HFE ( ) = IC/IB

Figs. C.2.c

****** GRAPHICS PLOT ******



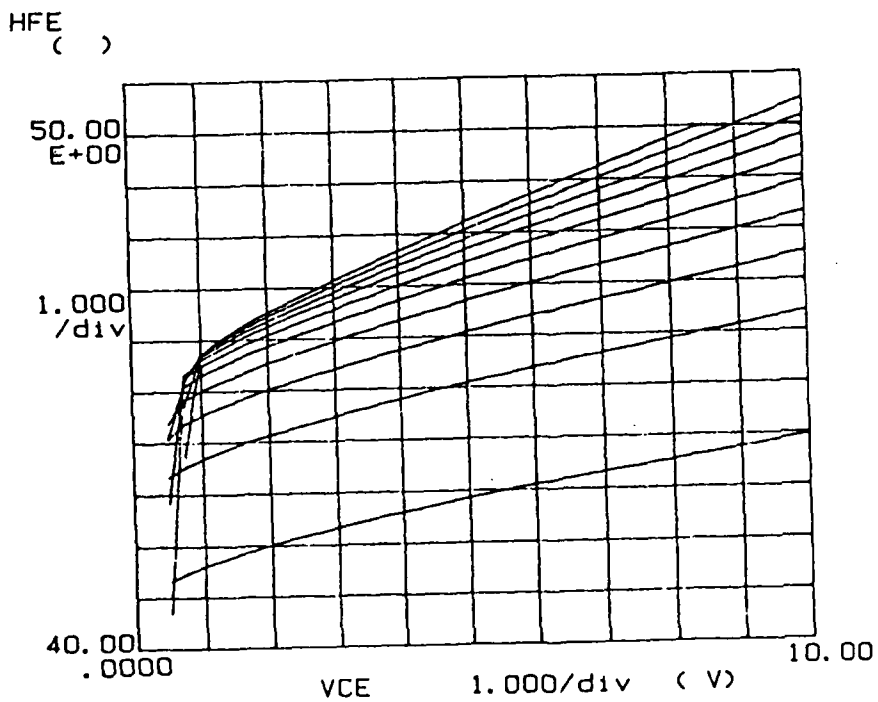
Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

Variable2:
IB -Ch2
Start .000 A
Stop 2.000mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



Variable1:
VCE -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2500V

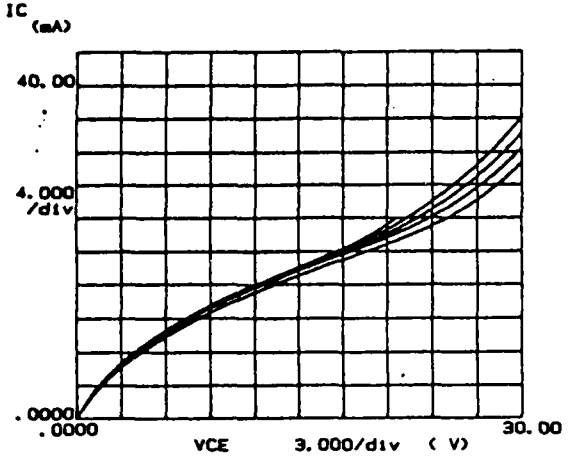
Variable2:
IB -Ch2
Start .000 A
Stop 2.000mA
Step 200.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

Figs. C.2.d

****** GRAPHICS PLOT ******



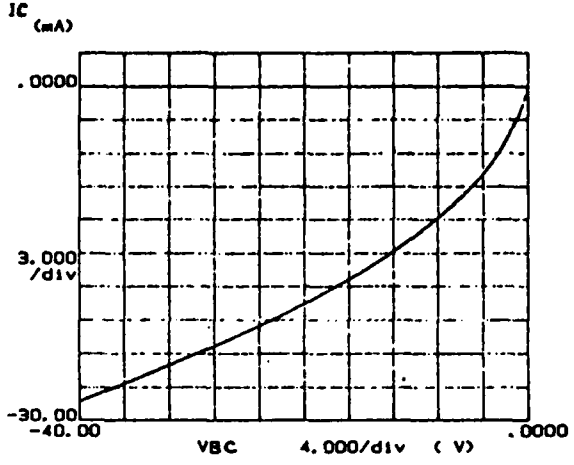
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VCE -Ch2
Linear sweep
Start .0000V
Stop 30.000V
Step .2500V

Variable2:
IB -Ch1
Start .000 A
Stop 2.000mA
Step 500.0uA

Constants:
VE -Ch1 .0000V

HFE ( ) = IC/IB

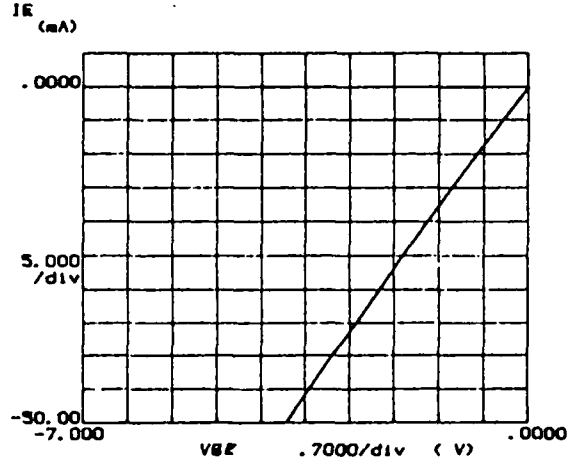
****** GRAPHICS PLOT ******



Variable1:
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Linear sweep
Start .0000V
Stop -40.000V
Step -.2000V

Constants:
V -Ch2 .0000V

****** GRAPHICS PLOT ******

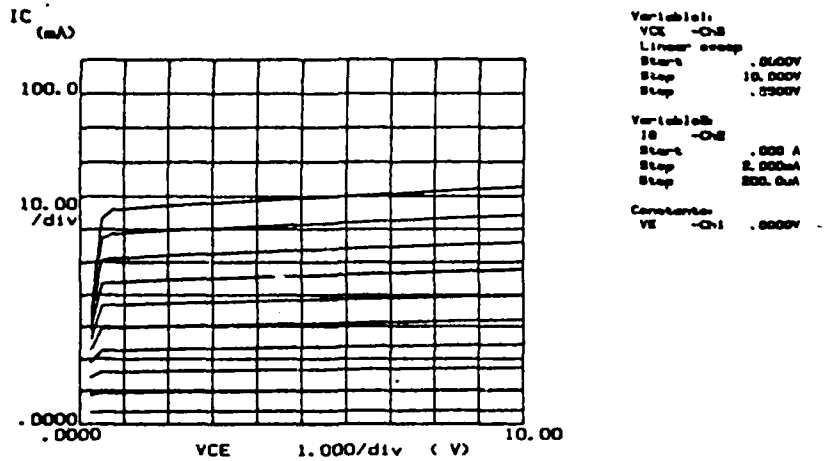


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Linear sweep
Start .0000V
Stop -7.0000V
Step -.0450V

Constants:
V -Ch2 .0000V

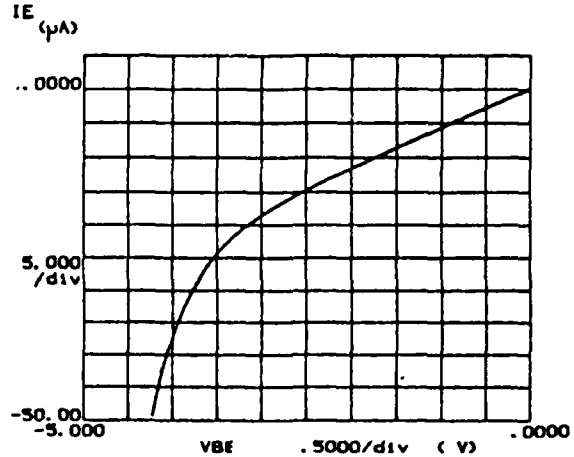
Figs. C.3.a

****** GRAPHICS PLOT ******

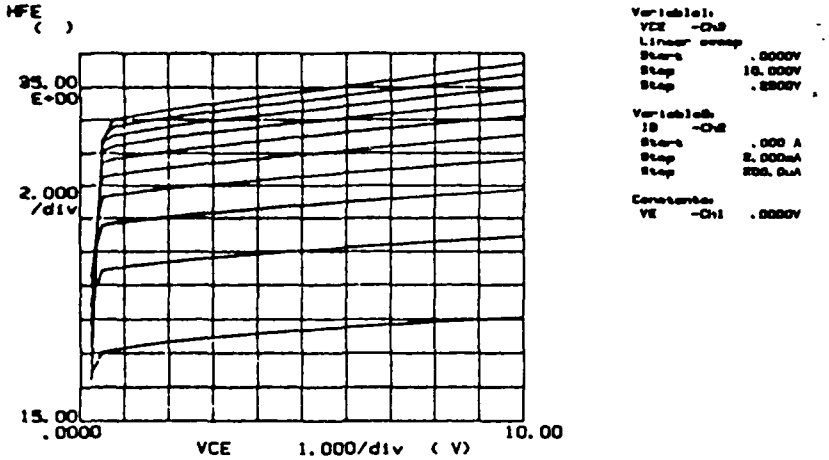


HFE ( ) = IC/IB

****** GRAPHICS PLOT ******

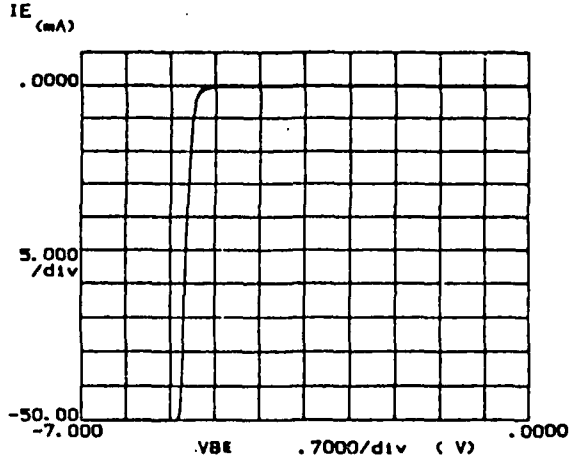


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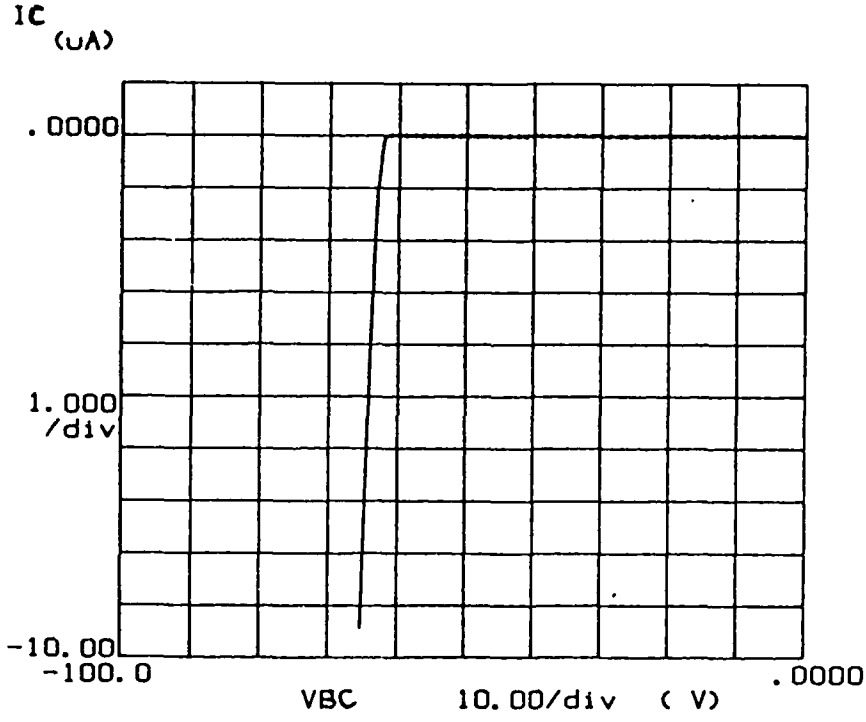


HFE ( ) = IC/IB

****** GRAPHICS PLOT ******



****** GRAPHICS PLOT ******

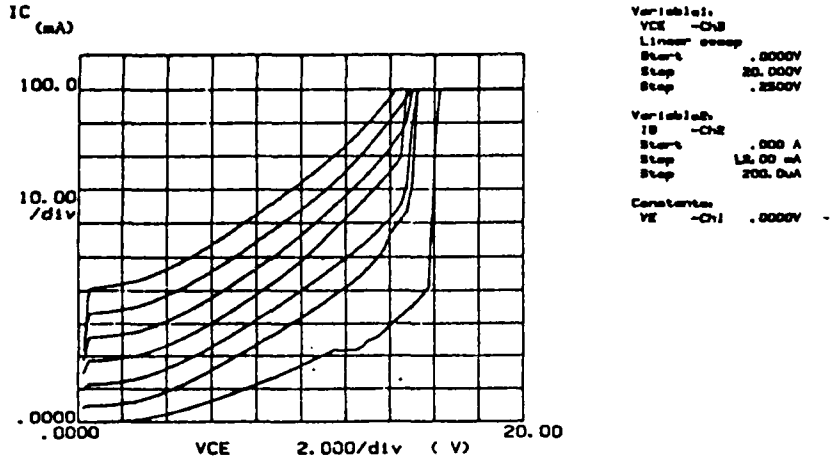


Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -100.00V
Step - .2000V

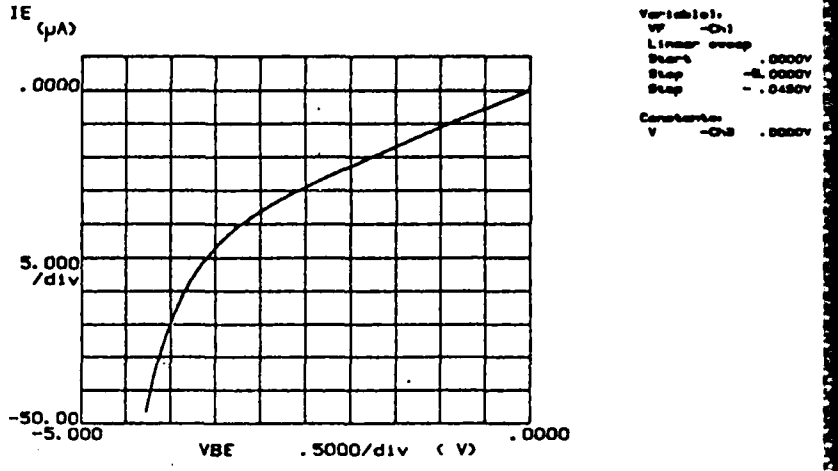
Constants:
V -Ch3 .0000V

Figs. C.3.c

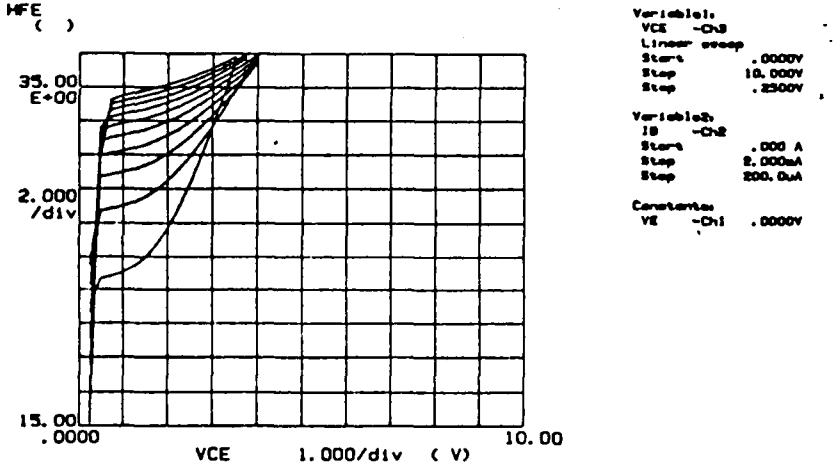
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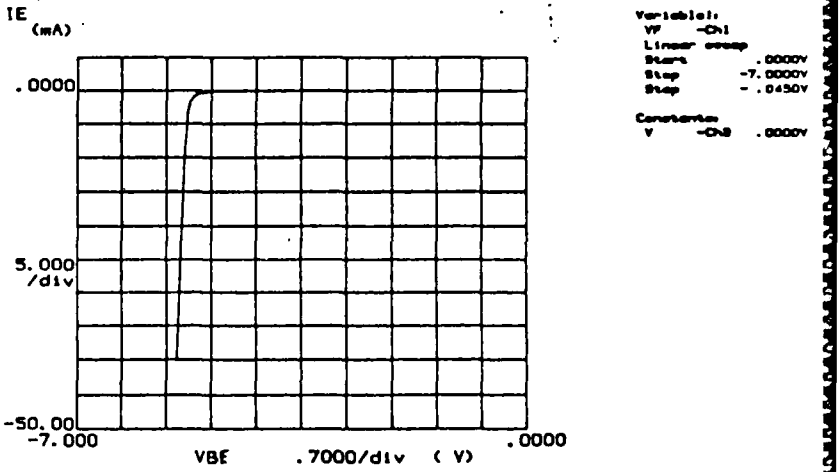
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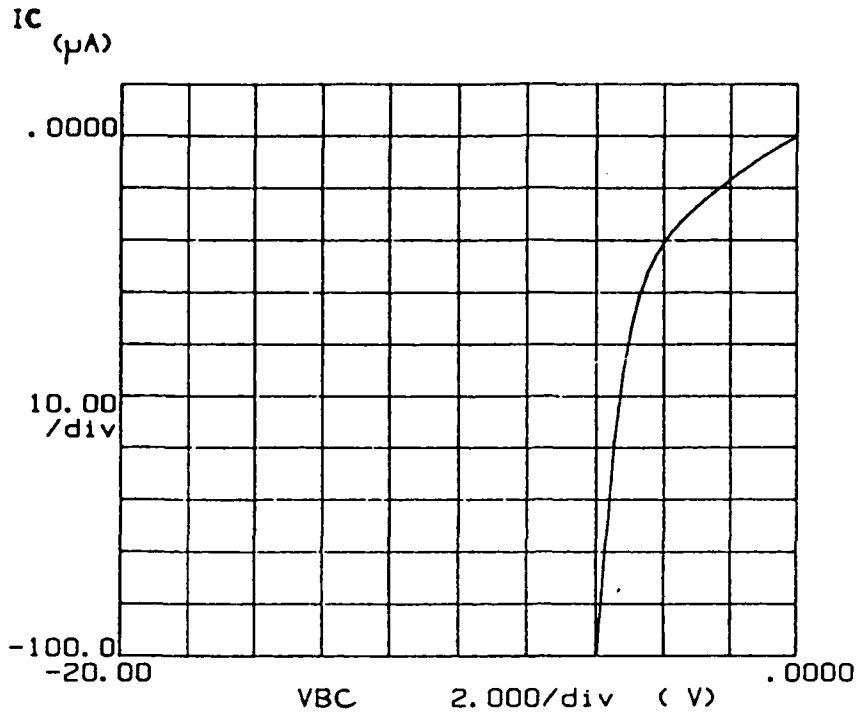
****** GRAPHICS PLOT ******



****** GRAPHICS PLOT ******



****** GRAPHICS PLOT ******



Variable1:
VF -Ch1
Linear sweep
Start .0000V
Stop -20.000V
Step - .2500V

Constants:
V -Ch3 .0000V

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18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Electrostatic Discharge (ESD), Static Bleed-off, Composite Materials, Dielectric Mixture

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A class of composites, popularly known as static dissipative materials, is widely used in semiconductor manufacturing and/or handling situations, as surface-finishes, packing media, etc. to prevent excessive triboelectric charge accumulation upon semiconductor

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devices, lest device failure may occur due to electrical overstressing. Presently, a mixture model to predict the effective electrostatic propensity of a two-phase composite formed by a dispersal of conducting (and shaped) inclusions in an insulating medium is developed on the basis of stochastical considerations. A closed-form expression to determine optimum design-value for the volume-fraction of conducting inclusions so as to get a minimum static bleed-off time, is derived. The optimization is done with the constraints imposed on the electrical resistivity of the composite by certain practical considerations.

Electrostatic Propensity and Bleed-off Characteristics of Composite Materials

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Rochester Institute of Technology

May 9, 1986
Rochester Hilton
175 Jefferson Road
Rochester, New York 14623

ABSTRACT

A class of composites, popularly known as static dissipative materials, is widely used in semiconductor manufacturing and/or handling situations, as surface-finishes, packing media, etc. to prevent excessive triboelectric charge accumulation upon semiconductor devices, lest device failure may occur due to electrical overstressing. Presently, a mixture model to predict the effective electrostatic propensity of a two-phase composite formed by a dispersal of conducting (and shaped) inclusions in an insulating medium is developed on the basis of stochastical considerations. A closed-form expression to determine optimum design-value for the volume-fraction of conducting

inclusions so as to get a minimum static bleed-off time, is derived. The optimization is done with the constraints imposed on the electrical resistivity of the composite by certain practical considerations.

INTRODUCTION

A variety of synthetic and organic composites are used in the industrial environment as bench-top materials, floor-finishes, containers, carpets/floor-mats, workroom apparel/garments, etc. and these materials, in general, are highly electrostatic propensive [1-5]. That is, whenever there are two nonconductive (insulating) materials moving in opposite directions abrading against each other, a high triboelectric potential would build up between the abrading surfaces on separation; as a result, electric charges of opposite polarity accumulate upon these surfaces and they do not bleed-off easily dúe to high resistivity of the insulating media. They can stay put upon the surfaces as puddles over a long duration of time until a conducting medium comes in contact with the surfaces [2].

In electronic industries triboelectricity is regarded as a menace [6] because any accidental static voltage transfer/buildup occuring in a semiconductor device may cause catastrophic or latent device-failure. Especially microelectronic devices pose high reliability problems arising from sneaky failures due to electrostatic discharge (ESD) which is considered as a new contaminant of the age of chips. One of the preventive measures adopted to control static electrification in microelectronic industries is to use a distinct class of synthetic composites which are less prone to triboelectric effects. Such static propensity-controlled composites are of two types, namely (i) antistatic or static-repulsive materials and (ii) static-dissipative or static-conductive materials [5].

Static-conductive composite materials help to solve the problems of

electrostatic discharge by controlling the generation, accumulation, and dissipation of static charges. They offer proven static protection in electronic manufacturing, assembly, and test areas -- in hospitals and in computer facilities where sensitive electronic equipment is installed and handled.

Static dissipative composites are, in general, composed of conductive materials (such as carbon, metallic particles, etc.) which are diffused into an insulating medium like ceramic, rubber or plastic, etc. The conductive elements are randomly distributed throughout the surface as well as in the bulk portion of the material so that a required amount of volume and surface electrical resistivity are realized, and this resistivity generally determines the ability of the material to dissipate the static charge. Though it can be expected that electrostatic decay performance would bear a linear relation with the conductivity, this hypothesis may not be wholly correct in respect of a composite material. This is because of the capacitance effects associated with the material which would "slow down" the charge dissipation rate.

The purpose of the present investigations is to develop a stochastical model which would predict the electrostatic propensity and bleed-off properties of a static dissipative composite in terms of quantifiable terms suitable for design calculations pertaining to the fabrication of composites having desired static-dissipative characteristics.

Stochastical characteristics of the test composite:

In order to design a composite medium which has a high electrostatic dissipative property, it is necessary to consider the electromagnetic response of the material in terms of both electrical conductivity and permittivity of the medium. For this purpose, the test composite is presently regarded as a two-phase stochastical mixture in which the insulating medium forms the dispersing continuum and the conducting phase constitutes the random inclusions.

The electrostatic propensity of this composite/mixture can be quantified in terms of electrical polarisability of the medium which depicts the surface density of bound charges therein. And the polarisibility can be assessed in terms of dielectric susceptibility or permittivity characteristics of the chaotic mixture. And, to quantify the static-bleed-off abilities of the test medium, one has to consider the resistivity of the medium which is primarily determined by the conducting inclusions.

To evaluate the effective permittivity and/or conductivity of the test material, the relevant parameters to be considered are therefore, (i) the permittivity (ε_1) and the conductivity (σ_1) of the dispersing inclusions, (ii) the volume-fraction of the inclusions (ϕ), (iii) the permittivity (ε_2) and conductivity (σ_2) of the dispersing insulator, and (iv) a shape-factor (g) depicting the geometry of the inclusions.

There are a host of formulas available in the literature [7] to

calculate the effective permittivity and/or conductivity of multiphase systems. However, they are based on the analytical formulation pertaining only to the material response to the electric field (Clausius-Mosotti principle) [7] and they do not consider the true statistical aspects of the mixture. The only stochastical formulation that exists is due to Lichtenecker [7] and Rother [8,9] and is known as logarithmic law of mixing. But even this logarithmic law has two deficiencies, namely (i) it has no dependency on the shape-factor (g) which is incorrect, and (ii) it would not reduce to a linear form so as to be inconsistent with certain limiting conditions as indicated by Reynold and Hough [10]. This inconsistency is due to an illogical supposition by Lichtenecker who considered a mixture as chaotic and ordered simulatneously [11].

Taking into view the aforesaid limitations on the existing mixture formulas, a generalized stochastical formulation applicable to any physical property of a mixture is presently derived by modifying the logarithmic law as indicated below:

Modified logarithmic law of mixing

Considering the theory of mixtures as a probability problem, Lichtenecker and Rother [8,9] deduced the logarithmic mixture law from general principles. For a mixture of two components, it is given by,

$$p = p_1^{\phi}\, p_2^{1-\phi} \tag{1}$$

where p depicts any generic physical property. Inasmuch as the logarithmic formulation is not consistent with Reynold-Hough's generalization on linearity [10], an alternate form of weighted

geometric mean, as given below, is proposed here:

$$p = C(p_1, p_2, \phi)\ p_U^{n(a/b)}\ p_L^{1-n(a/b)} \qquad (2)$$

where $p_U = \phi p_1 + (1-\phi)\ p_2$ and $p_L = [\phi/p_1 + (1-\phi)/p_2]^{-1}$ are the Weiner's upper and lower limits respectively. In Equation (2) it is presumed that n^{th} fraction of the chaotic system behaves as if oriented in the direction of the electric field induction and the remaining $(1-n)^{th}$ fraction is oriented orthogonally. Here, n is considered as a function of the axial ratio of the shaped-inclusions (namely a/b) only, and C is the weighting factor depending on p_1, p_2, and ϕ.

The expression of Equation (2) is, however, applicable to a statistical mixture only when the following constraints are met with: (i) In the limiting value of $n \to 1/2$, Equation (2) should degenerate to Equation (1). (ii) In order to satisfy the extreme conditions of a/b tending to infinity or zero, n(a/b) should be bounded within the limits $0 \leq n \leq 1$ for any values of p_1 and p_2 and for $0 \leq \phi \leq 1$. (iii) The magnitude of p (for any finite values of p_1 and p_2 and for $0 \leq \phi \leq 1$) should always be bounded and lie within Wiener's limits. (iv) At the terminal values of ϕ -- namely 0 and 1 -- the value of p should be entirely specified by the single component value, p_1 and p_2.

With the application of the aforesaid constraints, and after elaborate algebraic manipulations, Equation (2) can be explicitly given by the following expression(s):

$$
p = \begin{cases}
X(\phi)/2, \; p_1 > p_2, & 0 \le \phi < \phi_1; \\
Y(\phi)/2, \; p_1 < p_2, & \\
1/2 \left[\dfrac{A(\phi_1)}{2C(\phi_1)} + \dfrac{B(\phi_2)}{2C(\phi_2)} \right] \cdot C(\phi)\, Z(\phi), \; p_1 > p_2, & \phi_1 \le \phi < \phi_2; \\
1/2 \left[\dfrac{B(\phi_1)}{2C(\phi_1)} + \dfrac{A(\phi_2)}{2C(\phi_2)} \right] \cdot C(\phi)\, Z(\phi), \; p_1 < p_2, & \\
Y(\phi)/2, \; p_1 > p_2, & \phi_2 \le \phi \le 1 \\
X(\phi)/2, \; p_1 < p_2, &
\end{cases} \qquad (3)
$$

where $X(\phi) = Z(\phi) + 1/p_L(\phi)$, $Y(\phi) = Z(\phi) + p_U^n(\phi)$, $Z(\phi) = p_U^n(\phi) \; / \; p_L^{n-1}(\phi)$, $A(\phi) = 1 + 1/p_U^n \; p_L^n$, $B(\phi) = 1 + 1/p_U^{n-1} \; p_L^{n-1}$ and $C(\phi) = p_1^{\phi} \; p_2^{1-\phi} / \sqrt{p_L(\phi) \cdot p_U(\phi)}$.

Further, by implementing the constraint on the extremities of a/b ratio, the parameter n can be written explicitly as a function of a/b in the following manner:

$$
n = \frac{(5 - M)}{4} \qquad \text{if } p_1 \ge p_2 \qquad (4a)
$$

and

$$
n = \frac{(M - 1)}{4} \qquad \text{if } p_2 \ge p_1 \; . \qquad (4b)
$$

Here, M is a function of a/b ratio and is given by [12],

$$M = e^2 \left[1 - (1-e)^{\frac{1}{2}} \frac{\text{arc sin } (e)}{e} \right]^{-1} \tag{5}$$

where e is the eccentricity of the particle which can be expressed in terms of the axial ratio as follows:

$$e = \left(1 - \frac{b}{a}\right) \quad \text{if } a > b \tag{6a}$$

$$\text{and} \quad e = \left(\frac{a}{b} - 1\right) \quad \text{if } a < b. \tag{6b}$$

When e = o (which corresponds to the base of $\frac{a}{b} = 1$, or for spherical and sphere-like particles), the value of M becomes 3; and when $\frac{a}{b} >> 1$ or $\frac{a}{b} << 1$, M asymptotically reduces to unity. Hence, from Equation (4) it follows that

$$n\left(\frac{a}{b}\right)\Big|_{\frac{a}{b} = 1} = \frac{1}{2} \tag{7a}$$

$$n\left(\frac{a}{b}\right)\Big|_{\frac{a}{b} \to \infty \text{ or } 0} \begin{array}{l} = 1 \text{ or } 0 \text{ (if } p_1 > p_2); \\ = 0 \text{ or } 1 \text{ (if } p_1 < p_2). \end{array} \tag{7b}$$

Therefore, $n\left(\frac{a}{b}\right)$ is always within 0 to 1 limits, irrespective of the extent of particle eccentricity.

Further, it can be shown that the coefficient function C of Equation (2) attains minimum and maximum values at volume fractions of ϕ_1 and $\phi_2 = (1 - \phi_1)$ respectively; and ϕ_1 is given by

$$\phi_1 = \tfrac{1}{2} - \tfrac{1}{2}\sqrt{1 - 4t} \tag{8a}$$

where t can be explicitly stated as

$$t = \frac{(p_1 + p_2)}{2(p_1 - p_2)} \cdot \frac{1}{\ell n\left(\frac{p_1}{p_2}\right)} - \frac{p_1 p_2}{(p_1 - p_2)^2} \cdot \tag{8b}$$

Equation (3) represents a generalized expression which can quantify the effective property such as the electrical permittivity, magnetic permeability, electrical conductivity, thermal conductivity, diffusion constant, and elastic properties of a two-phase composite in terms of the corresponding properties of the mixture constituents and the shape and volume-fraction of the inclusions [13].

ELECTROSTATIC PROPENSITY AND BLEED-OFF CHARACTERISTICS

To study the electrostatic propensity and bleed-off characteristics of a test composite, the two electrical properties which are of interest are the permittivity (ε) and the conductivity (σ) of the mixture-state which can be quantified by Equation (3), by substituting ε or σ in the place of the general parametric quantity, namely p. When a composite medium with an effective permittivity ε is subjected to triboelectrification, the corresponding surface-charge (q_s) induction can be related to the electrical polarisation ($\bar{P}$) as follows:

$$q_s = \left|\bar{P}\right| = (\varepsilon - 1)\, \varepsilon_o \left|\bar{E}\right| \tag{9}$$

where ε_o is the free-space permittivity and $\bar{E}$ denotes the electrical field intensity associated with the triboelectric potential of the medium.

Hence, the electrostatic propensity arising from triboelectric polarisation is directly proportional to the dielectric constant or the effective permittivity of the composite (assuming that the two materials involved in the abrading process are identical); however, if the materials involved are dissimilar, the triboelectrification would depend on the ratio of the dielectric constants of the materials concerned. That is, the relative triboelectrification in the materials A and B can be specified as

$$\frac{\bar{P}_A}{\bar{P}_B} = \frac{(\varepsilon_A - 1)}{(\varepsilon_B - 1)} \cdot \qquad (10)$$

In view of the above considerations, it follows that materials with low effective permittivity are less susceptible for triboelectric propensity. This property should be duly considered in the design of static-conductive materials as described below.

Static conductive materials can be characterized by their high static-dissipative abilities. Quantitatively, the time-constant (τ) of static bleed-off can be regarded as an indicator of the static-dispensing nature of the test medium. This time constant τ can be expressed in terms of the effective values of permittivity (ε) and the electrical conductivity (σ) of the composite as follows:

$$\tau = \varepsilon_0 \varepsilon \; / \; \sigma \qquad (11)$$

where the values of ε and σ can be determined by Equation (3) and ε_0 is the free-space permittivity.

In order to achieve a fast bleed-off, the time constant τ must be minimum. However, minimization of τ is subjected to certain practical constraints. The constraints are: (i) The test composite is a stochastical mixture and therefore the effective values of ε and σ should be specified by the expression of Equation (3). (ii) The maximum value of the volume-fraction (ϕ) of the conducting inclusions is equal to 1. (iii) The minimum value of the volume-fraction (ϕ) (threshold value) is determined and limited by the amount of conducting inclusions required for the establishment of the electrical percolative current paths in the mixture-matrix. (iv) Considering a test material of cross-sectional area 'a' and length 'ℓ,' the resistance per unit length, namely $R/\ell = 1/\sigma a$, should be greater than a minimum value specified by certain mandatory rules concerning fire-hazard/short-circuit protection specifications stipulated for industrial applications of these materials [14]. With the aforesaid constraints, an optimum value for ϕ can be obtained by minimizing the bleed-off time-constant (τ) as detailed below:

The electrical capacity (C) and the resistance (R) of the test material of cross-sectional area 'a' and length 'ℓ' are given by

$$C = \varepsilon_0 \varepsilon \; a/\ell \qquad (12)$$

and

$$R = \ell/\sigma a. \tag{13}$$

And considering the fire-hazard /short-circuit protection limitations on the resistivity of a test material, the relevant constraint can be explicitly written as:

$$\rho_{min} \leq \frac{1}{\sigma} \tag{14}$$

where ρ_{min} is the minimum value of bulk resistivity of the composite material prescribed by fire-proof regulations [15].

Using Equation (3) and with relevant simplifications, the constraint specified by Equation (14) can be rewritten as

$$\phi_{min} < \phi < \frac{-\ell og_e\ (\rho_{min}\sigma_2)}{\ell og_e\ (\sigma_1/\sigma_2)} \tag{15}$$

where ϕ_{min} specifies the threshold value required for the current percolation.

Considering the time-constraint τ (equal to RC), its approximate value, determined by Equations (3) and (11), can be expressed as follows:

$$\tau = \varepsilon_o \left[\frac{\varepsilon_2}{\sigma_2}\right]^{1-\phi} \frac{1}{\sigma_1^{\phi}} . \tag{16}$$

Hence, to obtain a minimum value for τ, (i) ε_2 should be close to 1; and, (ii) since $\sigma_2 >> \sigma_1$, it is necessary to take the largest possible value of ϕ. Therefore, the design- value of ϕ (as given by Equation 15) should be

$$\phi = - \frac{\ell og_e (\rho_{min}\ \sigma_2)}{\ell og_e\ (\sigma_1/\sigma_2)} \ . \qquad (17)$$

DESIGN EXAMPLE

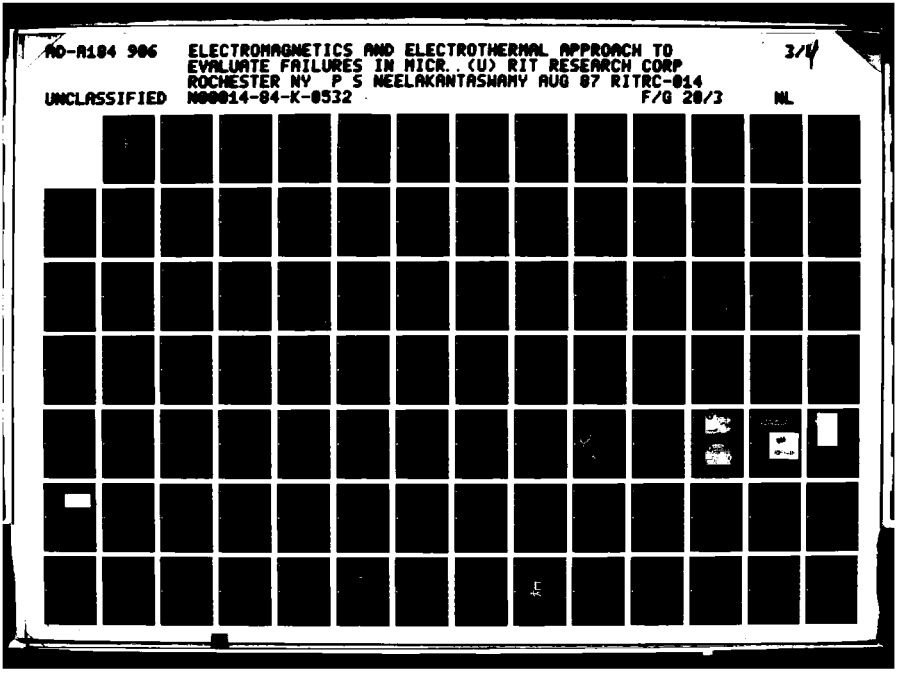
Consider a composite material formed by blending Bakelite and recycled aluminium powder. The Bakelite material (insulator) has the following values for the electrical constants: $\varepsilon_2 = 4.5$ and $\rho_2 = 2 \times 10^{14}$ ohm-meter; and for aluminium, $\varepsilon_1 = 1$ and $\sigma_2 = 3.53 \times 10^7$ Siemens/meter.

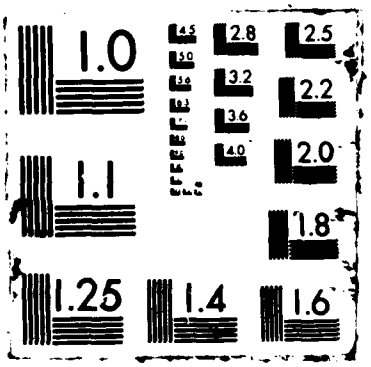
Suppose this composite material is used as a static-conductive floor covering. Then, it has to meet the electrical resistance requirements of the National Fire Protection Association Bulletin 56A, "Standard for the Use of Inhalation Anesthetics." This standard specifies that the average electrical resistance of an installed floor shall be between 25000 ohms and 10^6 ohms as measured between two electrodes placed 3-feet apart. The average resistance to ground shall be more than 25000 ohms as measured between a ground connection and an electrode placed at any point on the floor. The resistances represent the average of five or more readings per room or installation and are measured according

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1.0
1.1
1.25
1.4
1.6
2.8
2.5
3.2
2.2
3.6
2.0
4.0
1.8

to the procedures outlined in NFPA 56A which are essentially the same as that of ASTM F 150-72, "Standard Test Method for Electrical Resistance of Conductive Resilient Flooring."

Hence, taking the specified minimum value of 25000 ohms, the corresponding value of resistivity (ρ_{min}) of the test composite can be calculated by assuming the thickness of the floor covering as 1/8 inch. Then the calculated value of ρ_{min} is equal to 8×10^6 ohm-meter.

Using Equation (17), the optimum value of ϕ can be determined. In the present example, it is equal to 0.3386. The corresponding value of decay time-constant τ is 191.53μ sec. This value is acceptable as per MIL-B-81705B specification which stipulates a decay rate of 2.0 seconds as maximum.

The static decay time-constant (τ) of materials is normally measured by the procedures outlined in Method 4046 of Federal Test Method 101B, dated 8/15/74. The static accumulation or propensity can be determined similar to the test procedure of AATCC-134, "Electrostatic Propensity of Carpets." (or ANSI-ASTM D 2679-73 [15].)

STATIC PROPENSITY OF COMPOSITES WITH FIBROUS CONDUCTING INCLUSIONS

The present analysis can also be extended to composite materials formed by adding fibrous conducting inclusions in an insulating medium. Such composites would give a required extent of electrical

conductivity in a preferred direction determined by the orientation of the fibers. Using Fricke's formulation (described by one of the authors elsewhere [12]), Equation (3) can be simplified for long (or needle-like) fibrous inclusions. Relevant investigations are in progress.

RESULTS AND CONCLUDING REMARKS

The present work essentially describes, via appropriate modeling, a design methodology for choosing the correction composition of materials in the fabrication of static-conductive composites.

The relative electrostatic propensity of two materials (A and B) can be specified in terms of their dielectric constants (ε_A and ε_B) (Equation 10) as illustrated in Figure 1. For identical materials ($N = \varepsilon_A/\varepsilon_B = 1$), the charge propensity is the same in either of them as expected; and for large values of the dielectric constants of any one of the materials (say, ε_A), the relative propensity approaches asymptotically the ratio of the dielectric constant, namely N, irrespective of the magnitude of N. However, for low values of ε_A, the relative propensity tends to infinity for any given value of N. Therefore, it follows that, when a material of low permittivity abrades with a material of higher permittivity, the triboelectrification would be intense. This is true for composite materials also.

Considering the design of a composite with controlled static propensity, the choice of optimum value of volume-fraction (ϕ) (with the constraint on resistivity specified by fire-hazard limitations)

depends on both the conductivity of the inclusions as well as on the ratio of the conductivities of the dispersing insulator and the dispersed inclusions (Equation 17). Figure 2 illustrates the typical ranges of the practical values of the material constraints and the corresponding design-values of the volume-fractions.

If low volume-fraction of inclusions is preferred (so as to obtain, for example, certain desired mechanical/elastic properties), then as could be inferred from Figure 2 it is necessary to choose the dispersing material with higher conductivity. Thus the present formulation has a design flexibility to suit the practical situations.

Bleed-off time of a composite material as a function of conductivity of dispersed inclusions is presented in Figure 3 for two different volume-fractions of the inclusions. The delay or capacitive effects of the dispersing insulating medium is determined by the dielectric constant (ε_2), and Figure 3 corresponds to a (practical) parametric value of ε_2/σ_2 equal to 10^{15} ohm-meter. It can be observed from Figure 3 that both σ_1 and σ_2 control the bleed-off time to a significant extent and that the role of ε_2 is implicit. However, compatible design can be achieved as illustrated by an example given before as regards a mixture composite of Bakelite and aluminium powder.

Thus, the present work considers cohesively all the effective parameters which decide the bleed-off and static propensity properties of a composite material, and its utility in the design of static

dissipative composites needs no emphasis. Special composite dielectrics using rubber [6] as the insulator and solid electrolytes [17] as inclusions are being designed as per the present investigations.

ACKNOWLEDGEMENTS

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CAPTIONS FOR DRAWINGS:

Figure 1. Relative electrostatic propensity of two abrading (nonconducting) materials A and B. The magnitude of relative propensity is decided by the electrical polarisability/susceptibility of the materials quantified in terms of the permittivities ε_A and ε_B.

Figure 2. Dependency of the optimized volume-fraction on the conductivities of the dispersing insulator (σ_2) and the dispersing inclusions (σ_1). The range of values of σ_1 and σ_2 indicated correspond to practical materials; and the resistivity of a composite is limited to a minimum value of $\rho_{min} = 8 \times 10^6$ ohm-meter (as decided by fire-hazard regulations).

Figure 3. Bleed-off time of a test composite as a function of the conductivity (σ_1) of inclusions in the insulator for two typical volume-fractions (ϕ). The capacitive effects of the insulator are implicitly decided by the ratio ε_2 taken as a constant parameter. (The ranges of the constants depicted correspond to practical materials.)

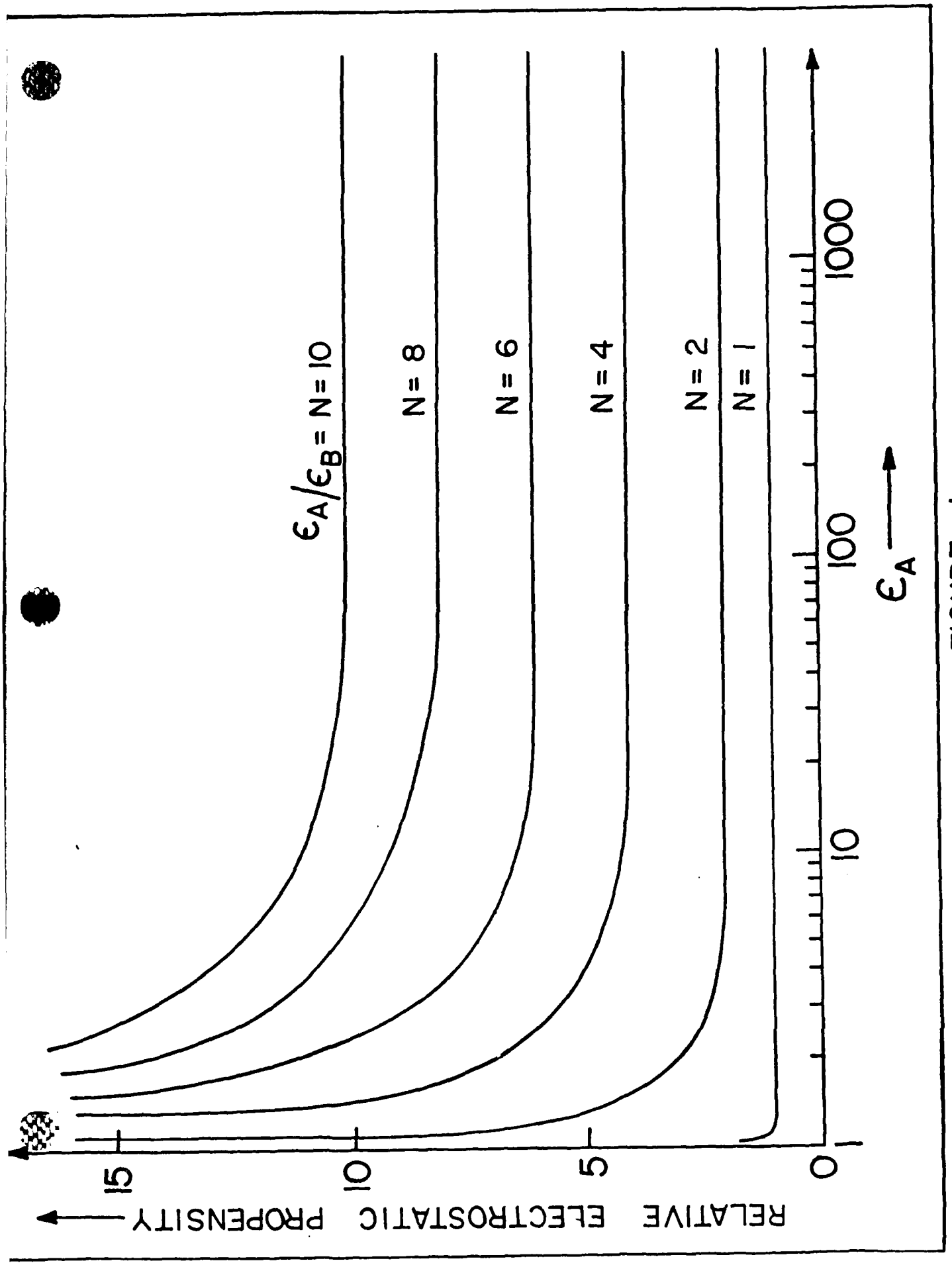

RELATIVE ELECTROSTATIC PROPENSITY
0
5
10
15
1
10
100
1000
ϵ_A
ϵ_A/ϵ_B= N= 10
N= 8
N= 6
N= 4
N= 2
N= 1

FIGURE 1

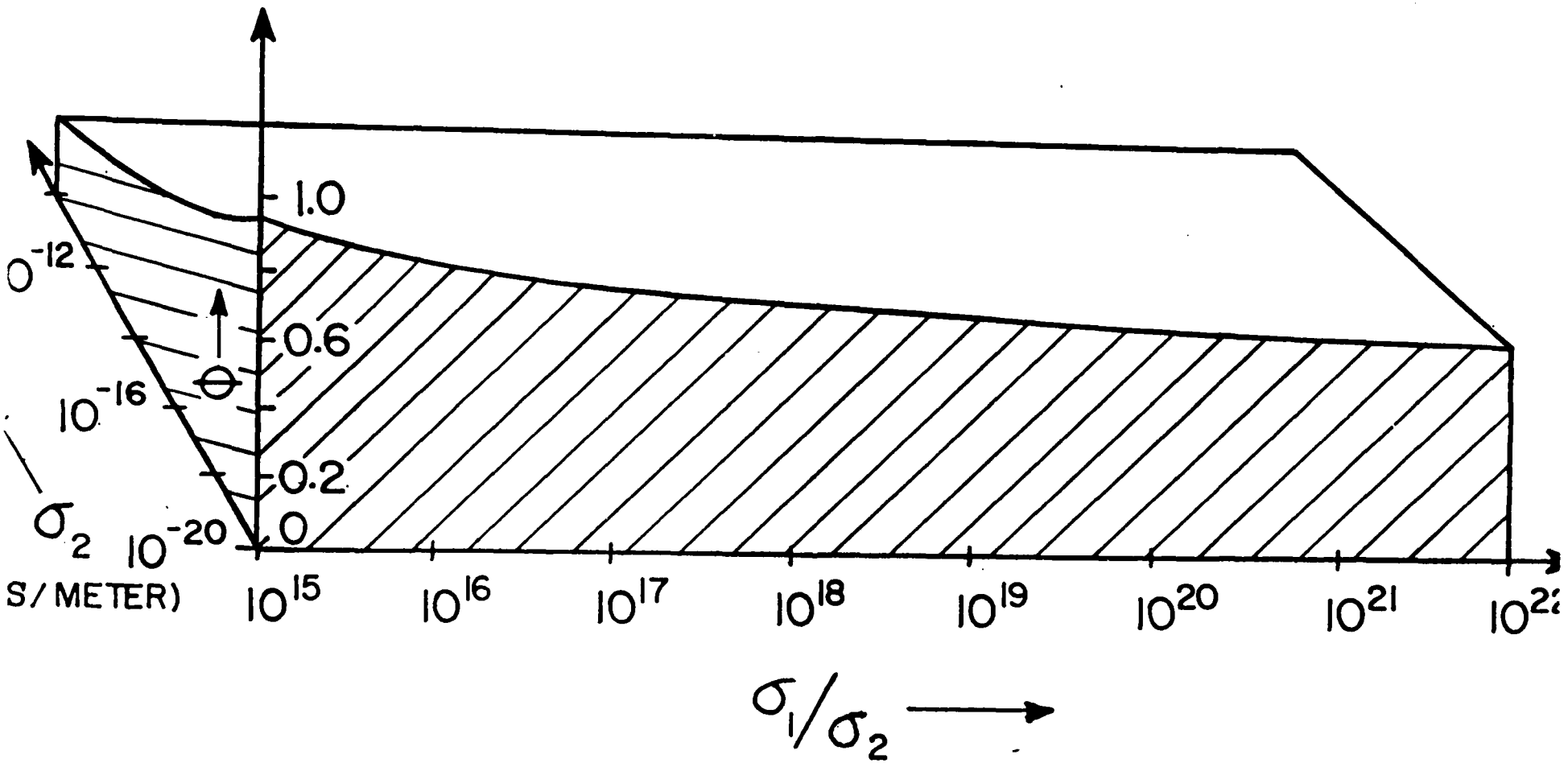

1.0
0.6
0.2
0
θ
10^{-12}
10^{-16}
10^{-20}
σ_2
S/METER)
10^{15}
10^{16}
10^{17}
10^{18}
10^{19}
10^{20}
10^{21}
σ_1/σ_2

FIGURE 2

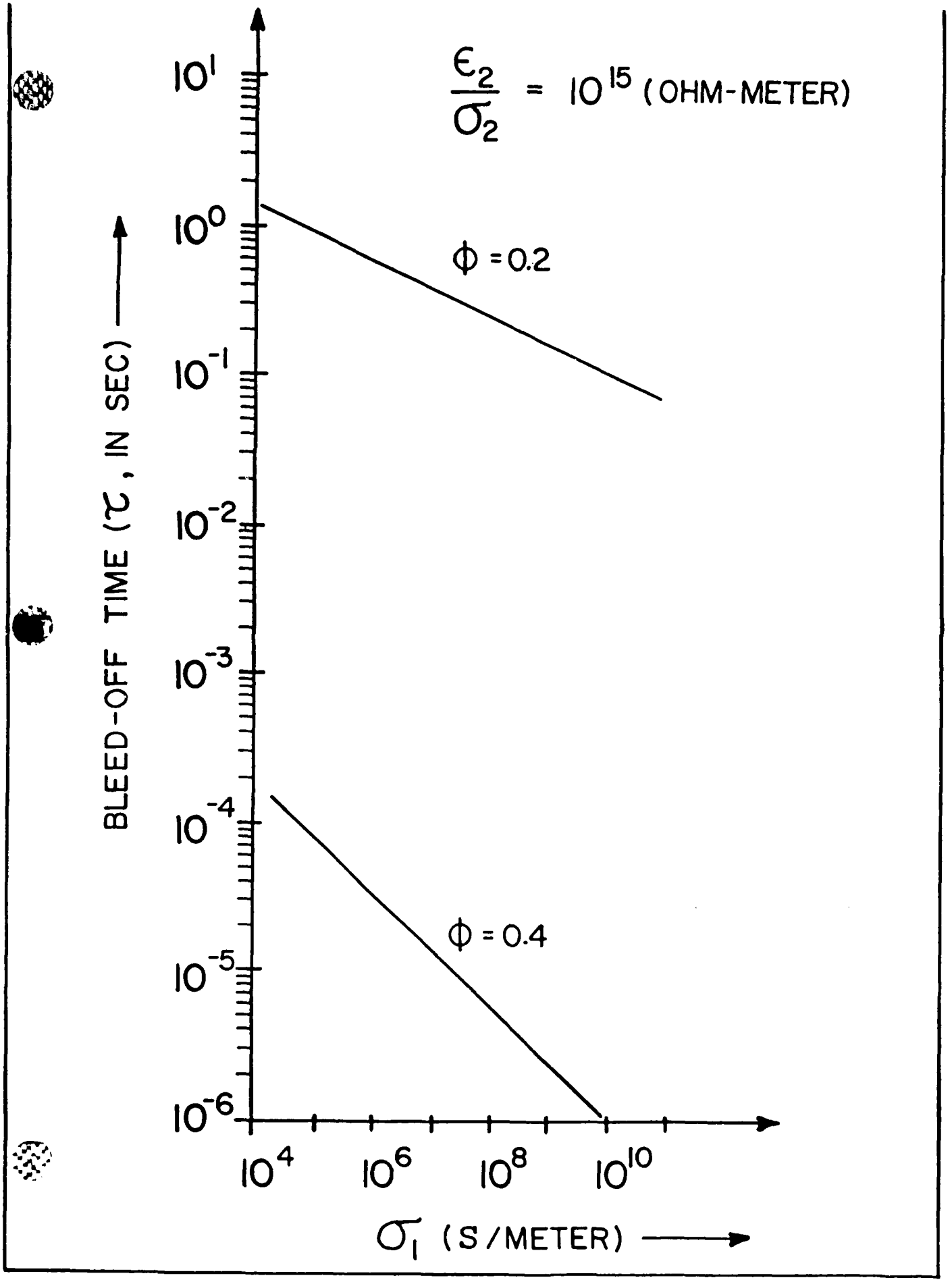

$\frac{\epsilon_2}{\sigma_2} = 10^{15}$ (OHM-METER)
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
BLEED-OFF TIME (τ, IN SEC)
$\phi = 0.2$
$\phi = 0.4$
10^{4}
10^{6}
10^{8}
10^{10}
σ_1 (S/METER)

FIGURE 3

COMPLEX PERMITTIVITY OF A DIELECTRIC MIXTURE: CORRECTED VERSION OF LICHTENECKER'S LOGARITHMIC LAW OF MIXING

Indexing terms: Dielectrics, Complex permittivity of a mixture, Lichtenecker's formula, Logarithmic law

Lichtenecker's logarithmic expression for the permittivity of a dielectric mixture is corrected to eliminate certain mathematical inconsistencies. This is done by a weighted geometric mean technique which renders the expression compatible with the so-called Reynold–Hough linear formulation. Calculated results are compared with some available data.

Introduction: Calculation of electrical induction in a dispersed system by classical electrostatic techniques forms the basis of the existing analytical descriptions of mixture dielectrics. The permittivity of a mixture (ε_s) is usually expressed in terms of the permittivity of the inclusions (ε_{1s}) and that of the dispersing continuum (ε_{2s}). (The suffix s here denotes the static field conditions.) The interrelation between the permittivities would also include the volume fraction ϕ of the inclusions and a 'field-ratio' term[1] to account for the depolarisation effects[1] governed by the shape and spatial distribution of the inclusions.

Reynold and Hough[1] succeeded in 1957 in reducing all the mixture formulations then available to the closest approximation of a linear form except for the so-called 'logarithmic law of mixing' developed by Lichtenecker and Rother.[2,3] They doubted some error in the logarithmic formulation and later (in 1974) Dukhin[4] attributed the observed inconsistency to an illogical assumption by Lichtenecker,[2,3] who considered a disperse system as chaotic and ordered simultaneously.

Despite the prevalence of the aforesaid mathematical inconsistency, the logarithmic law of mixing has surprisingly gained recognition, supported by experimental data gathered on chaotic mixtures with near-spherical inclusions.[5–7] However, it is still preferable to eliminate the persisting incompatibility of the logarithmic law with respect to the generalised linear form.[1] This could be done by the modifications suggested below.

Theoretical formulation: Considering a chaotic mixture, the effective permittivity as given by the logarithmic law of mixing corresponds to a weighted geometric mean[2,3] of ε_{1s} and ε_{2s}, namely $\varepsilon_s = \varepsilon_{1s}^{\phi}\varepsilon_{2s}^{\phi}$.

Inasmuch as the logarithmic relation is inconsistent, a different form of weighted geometric mean, as given below, is proposed:

$$\varepsilon = C(\varepsilon_1, \varepsilon_2, \phi)\varepsilon_U^{n(a/b)}\varepsilon_L^{1-n(a/b)} \tag{1}$$

where $\varepsilon_U = \phi\varepsilon_1 + (1-\phi)\varepsilon_2$ and $\varepsilon_L = [\phi/\varepsilon_1 + (1-\phi)/\varepsilon_2]^{-1}$ are Wiener's upper and lower limits, respectively. In eqn. 1, it is presumed that the nth fraction of the chaotic system behaves as if polarised in the direction of the electric field induction, and the remaining $(1-n)$th fraction is polarised orthogonally. Here, n is considered as a function of the axial ratio of the inclusions (namely, a/b) alone and C is the weighting factor depending on ε_1, ε_2 and ϕ.

The expression of eqn. 1 should satisfy certain limiting conditions pertaining to n, ϕ and ε. The conditions are: (i) $0 \le n \le 1$; (ii) $0 \le \phi \le 1$ and (iii) for any finite values of ε_1 and ε_2, ε must be bounded and lie within Wiener's limits. Hence

$$\varepsilon = \begin{cases} \left.\begin{matrix} X(\phi)/2, \varepsilon_1 > \varepsilon_2 \\ Y(\phi)/2, \varepsilon_1 < \varepsilon_2 \end{matrix}\right\} & 0 \le \phi \le \phi_1 \\ \dfrac{1}{2}\left[\dfrac{A(\phi_1)}{2C(\phi_1)} + \dfrac{B(\phi_2)}{2C(\phi_2)}\right]C(\phi)Z(\phi), \varepsilon_1 > \varepsilon_2 & \\ \qquad\qquad \phi_1 \le \phi \le \phi_2 & (2) \\ \dfrac{1}{2}\left[\dfrac{B(\phi_1)}{2C(\phi_1)} + \dfrac{A(\phi_2)}{2C(\phi_2)}\right]C(\phi)Z(\phi), \varepsilon_1 < \varepsilon_2 & \\ \left.\begin{matrix} Y(\phi)/2, \varepsilon_1 > \varepsilon_2 \\ X(\phi)/2, \varepsilon_1 < \varepsilon_2 \end{matrix}\right\} & \phi_2 \le \phi \le 1 \end{cases}$$

where $X(\phi) = Z(\phi) + 1/\varepsilon_L(\phi)$, $Y(\phi) = Z(\phi) + \varepsilon_L(\phi)$, $Z(\phi) = \varepsilon_U^n(\phi)/\varepsilon_L^{n-1}(\phi)$, $A(\phi) = 1 + 1/\varepsilon_U^n\varepsilon_L^n$, $B(\phi) = 1 + 1/\varepsilon_U^{n-1}\varepsilon_L^{n-1}$ and $C(\phi) = \sqrt{[\varepsilon_L(\phi)/\varepsilon_U(\phi)]}\varepsilon_1^{\phi}\varepsilon_2^{1-\phi}$.

Further, n is equal to $(5-M)/4$ or $(M-1)/4$, depending on $\varepsilon_1 > \varepsilon_2$ or $\varepsilon_1 < \varepsilon_2$, respectively. Here, M is a function of the a/b ratio which can be determined in terms of the eccentricity of the inclusions as indicated in Reference 7.

In eqn. 2, ϕ_1 and $\phi_2 = (1-\phi_1)$ denote the volume fractions at which the weighting coefficient C attains minimum and maximum values, respectively; and it can be shown that

$$\phi_1 = \tfrac{1}{2} - \tfrac{1}{2}\sqrt{(1-4t)} \tag{3}$$

where t is given by

$$t = \frac{(\varepsilon_1+\varepsilon_2)}{2(\varepsilon_1-\varepsilon_2)\ln(\varepsilon_1/\varepsilon_2)} - \frac{\varepsilon_1\varepsilon_2}{(\varepsilon_1-\varepsilon_2)^2} \tag{4}$$

Results and conclusions: Since eqn. 2 is in a linear form and is functionally related to the shape-dependent (depolarising) parameter a/b, it is compatible with Reynold–Hough's expression. It is also valid for dynamic (time-varying) cases relevant to the complex permittivity of a mixture.

Table 1 COMPARISON OF CALCULATED DATA ON THE PERMITTIVITY OF A DIELECTRIC MIXTURE

Volume fraction, ϕ		0	0·1	0·2	0·3	0·4	0·5	0·6	0·7	0·8	0·9	1·0
a/b ratio	Calculated by:	Dielectric constant of mixture (ε_s) (Mixture constituents: $\varepsilon_1 = 78{\cdot}3$, $\varepsilon_2 = 2{\cdot}0$)										
1·0	Lichtenecker's formula[2]	2·00	2·89	4·17	6·01	8·67	12·51	18·06	26·06	37·60	54·26	78·3
	Present method	2·00	2·89	4·17	6·01	8·67	12·51	18·06	26·06	37·60	54·26	78·3
	Boned & Peyrelasse formula[8]	2·00	3·02	4·25	5·00	7·50	11·00	17·01	26·96	40·52	58·3	78·3
5·0	Lichtenecker's formula[2]	—	—	—	—	—	—	—	—	—	—	—
	Present method	2·00	4·32	6·00	9·06	13·43	19·53	27·96	39·27	53·70	58·91	78·3
	Boned & Peyrelasse formula[8]	2·00	4·36	6·42	8·41	12·46	19·25	27·27	37·90	50·16	64·17	78·3
0·1	Lichtenecker's formula[2]	—	—	—	—	—	—	—	—	—	—	—
	Present method	2·00	4·7	6·60	10·29	15·41	22·49	32·09	44·63	59·00	61·97	78·3
	Boned & Peyrelasse formula[8]	2·00	5·70	8·41	11·52	17·44	25·67	35·94	48·23	58·20	68·02	78·3

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To verify the present formulation, theoretical results on the permittivity obtained by a recent technique of Bonnet and Peyrelasse[8] for a typical dispersed system are presented in Table 1 along with the results due to the present and logarithmic formulations. The formulation of Bonnet and Peyrelasse[8] is rigorous but involves elaborate integrations in computing the results. Comparable results can, however, be obtained with ease by the present formulation which is in closed form (eqn. 2).

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IMPATT diodes are useful as high peak-power microwave sources intended for short duration applications such as in missile-borne systems. However, they exhibit high-catastrophic failures indicated by either peripheral (mesa surface) burnouts or by intense filamentary shortcuts within the bulk of the semiconductor. Such failures are normally attributed to electrical overstressings (EOS) arising from RF-associated transients or perturbations due to changes in bias voltage, RF-impedance

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These electrical overstressings significantly influence the temporal and spatial thermal response of the device leading to the provocation of catastrophic failures. Hence in order to obtain optimum utility yield of IMPATTs, failure-prediction and trade-off studies required for design-reviews are considered here by identifying the mechanisms of failures along with relevant heat-flow calculations (Wunsch-Bell approach) compatible with the diode geometry and electrothermal power relations. For a given extent of failure propensity due to thermal runaway reliability aspects of some typical diode structures are evaluated.

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FILAMENTARY HOT-SPOTS IN MICROWAVE IMPATT DIODES: MODIFIED WUNSCH-BELL MODEL

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Summary

IMPATT diodes are useful as high peak-power microwave sources intended for short duration applications such as in missile-borne systems. However, they exhibit high-catastrophic failures indicated by either peripheral (mesa surface) burnouts or by intense filamentary shortcuts within the bulk of the semiconductor. Such failures are normally attributed to electrical overstressings (EOS) arising from RF-associated transients or perturbations due to changes in bias voltage, RF-impedance loading and/or due to external stimuli such as electrostatic discharge (ESD), electromagnetic pulsing (EMP), etc. These electrical overstressings significantly influence the temporal and spatial thermal response of the device leading to the provocation of catastrophic failures. Hence in order to obtain optimum utility yield of IMPATTs, failure-prediction and trade-off studies required for design-reviews are considered here by identifying the mechanisms of failures along with relevant heat-flow calculations (Wunsch-Bell approach) compatible with the diode geometry and electrothermal power relations. For a given extent of failure propensity due to thermal runaway reliability aspects of some typical diode structures are evaluated.

Introduction

Modern high performance radars and missile-borne systems require microwave solid-state sources capable of delivering high peak-powers at maximum efficiency, together with the adjunct requirement of high performance reliability. IMPATT diodes are useful in such applications, but they exhibit significant susceptibility to catastrophic failures arising from electrical overstresses (EOS) caused by electrical transients/perturbations due to undesirable external influences,[1] such as ESD, EMP, etc., or from circuit-associated changes like bias-voltage fluctuations or RF-impedance ("detuning") effects[2], etc. Proneness to such failures of IMPATTs is due to the diodes being operated close to their electrical and thermal limitations so as to realize high RF power output and maximum efficiency. Typically, input power densities of IMPATTs are in the 10^4 W/cm^2 range under CW operation; and they approach 10^5 W/cm^2 under pulsed operations with pulse durations of several microseconds at duty cycles in the range of 10 to 40%.

In order to improve the yield of less failure prone IMPATT diodes so as to make them cost-effective when used in high reliability systems, it is necessary to understand thoroughly the failure mechanism(s) involved so that appropriate corrective measures can be adopted at the design-level.

The available fault-isolation data from failed diodes[3-5] indicate metal penetration from contacts into the semiconductor and/or burnout sheaths and cracks along the mesa periphery. Although the damage sites usually show shapeless, large-area metal precipitates, well-defined metallic filaments indicating the existence of elongated hot-spots in the core have also been identified in some instances[3]. The catastrophic appearances of such filamentary hot-spots originate from the nonuniform temperature distribution across the diode resulting from finite thermal spreading resistance of the diode/heat-sink combination. Normally, the edge regions of the diode are cooler than the inner ones. Further, since both the saturation current and the avalanche multiplication factor are heavily dependent on local junction temperature, the resulting current density profile would invariably be nonuniform.

Under normal operating conditions, the negative temperature coefficient of the avalanche multiplication process would dominate the positive temperature coefficient of the saturation current. Consequently, the cooler regions of the diode would carry more current than the warmer parts. This overall negative temperature coefficient of the current density stabilizes the diode against the thermal runaway. That is, any local increase in temperature would cause the current and hence the power dissipation to drop at that point, bringing the temperature downward.

However, with the changes in input power, this stabilization of current distribution within the diode will be upset by either one of the following situations:

(i) The temperature build-up in the warmer (inner) parts of the diode allowing the saturation current to dictate the local current flow and power dissipation, and

(ii) large current densities in the cooler (outer) parts of the diode may induce a current-controlled bulk negative resistance[7-10] via space-charge effects associated with the generated carriers.

Both of these perturbation phenomena would ultimately lead the diodes to catastrophic failures. Changes in input power causing the aforesaid perturbation(s) may arise from external stimuli, such as electromagnetic pulsing (EMP), electrostatic discharge[1] (ESD), etc., or from circuit-associated instabilities provoked by bias-voltage fluctuations and/or by "detuning" effects[2] related to RF impedance loading.

In general, perturbations responsible for electrical overstressing would be transient in nature. Therefore, the relevant failure mechanisms would be studied by temporal and spatial electrothermal modeling of the diode/heat-sink combination and the criteria for failure should be established via thermal runaway/heat-flow formulations (Wunsch-Bell[11] approach).

Considering the destabilization of current distribution due to temperature build up in the warmer/core regions of the diode, Olson[3] developed an one-dimensional model which computes the d.c. J-V characteristics of Schottky-barrier IMPATT diodes for a pecified heat-sink thermal resistance. The characteristics displayed regions of initial increase and later decrease in positive differential resistance (PDR) followed by a region of current-controlled negative

differential resistance (NDR). Olson associated the formation of high current density filaments with the presence of not only the NDR, but also with that of the decreasing PDR. Indeed, experimental aspects of his study did indicate device failures for operating conditions of decreasing PDR. To explain such failures Olson[3] resorted to and extended the "phenomenological" argument of Sze[12] regarding the formation of a high-current filament even before the resistance of a diode going negative. According to Olson, the argument as applied to an IMPATT diode would go as follows: suppose the diode current is uniform and the diode resistance is positive but is dropping with increasing diode voltage (and electric field). Now, suppose that the electric field is also momentarily perturbed upward at some locale in the diode. This would cause the resistance at that point to drop and more current to flow through that point. By virtue of current continuity, the low-resistance high-current region will grow into a complete filament along the direction of current flow.

This argument of Olson[3] is not justifiable because a local increase in the field intensity would enhance the current flow at that point as long as the IMPATT operates in the PDR region, no matter whether PDR decreases or not. That is, local changes in the field cannot be applied selectively to the decreasing PDR region alone in order to explain the observed failures. Moreover, Olson's model[3], which is one-dimensional, bears an inherent assumption of uniform radial current and temperature distributions. Therefore it does not form a natural basis to explain the two-dimensional current filamentation extending in the radial and longitudinal directions.

Hence, in the present investigations a comprehensive two-dimensional (numerical) model to describe the local current density variations with changes in input power is developed which is devoid of the inconsistencies present in the Olson's phenomenological approach.[3,12]

Numerical Model

In the proposed model, the d.c. I-V characteristics of a Schottky-barrier IMPATT diode is evaluated via algorithmic description of the variations (spatial) in the current density as functions of input power. Numerical computation of the local current density is done using expressions relevant to thermionic emission current and avalanche multiplication factor, M.

The specific geometries of the diode considered here are illustrated in Figures (1a) and (1b). They represent cylindrical and annular ring mesa[13] structures, respectively. Further, the heat-sinks in Figures (1a) and (1b) are taken to be sufficiently large so that constriction effects are ignored. For a d.c. voltage applied to the diode, the resulting current and temperature profiles are determined as detailed below.

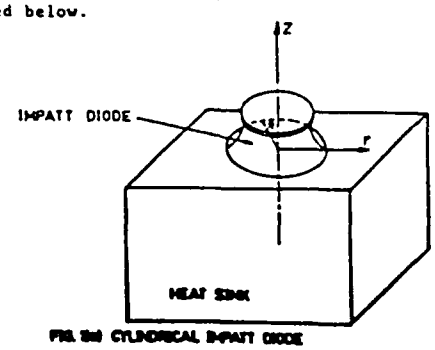


FIG. 1(a) CYLINDRICAL IMPATT DIODE

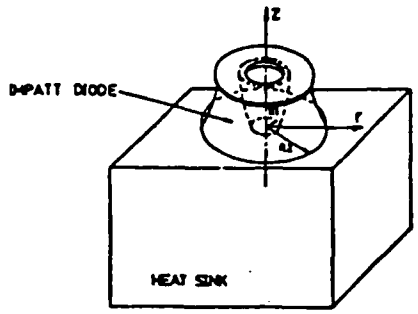


FIG. 1(b) ANNULAR RING IMPATT DIODE

Cylindrical Mesa Diode

Considering the diode structure depicted in Figure (1a), a uniform power density (P) profile is initially assumed over the diode cross-section. When a disk-shaped region (cylindrical diode) is placed over an infinitely large heat-sink and dissipating power uniformly across its cross-section, Laplace equation, for the spatial temperature distribution has a closed form solution for the region $z \leq 0$. In the $z = 0$ plane, this solution is given by[14,15]

$$T(r,0) = P\frac{R}{k_H}\frac{2}{\pi}E(m) + T_A, \quad 0 \leq r \leq R; \tag{1}$$

and

$$T(r,0) = P\frac{R}{k_H}\frac{2}{\pi}m^{\frac{1}{2}} \cdot$$

$$\left[E\left(\frac{1}{m}\right) - \left(\frac{m-1}{m}\right)K\left(\frac{1}{m}\right)\right] + T_A, \quad r \geq R, \tag{2}$$

where k_H is the thermal conductivity of the heatsink, T_A is the ambient temperature, $m = (r/R)^2$ and $K(m)$ and $E(m)$ are complete elliptic integrals of the first and second kind, respectively. The resulting temperature profile presents a maximum at the center of the disk and decreases with, r (Figure 2a).

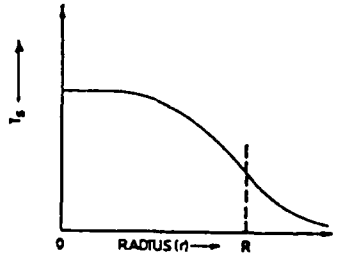


FIG. 2(a) TEMPERATURE PROFILE AT THE TOP SURFACE OF THE HEAT SINK (CYLINDRICAL DIODE)

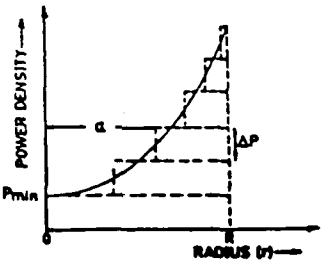


FIG. 2(b) POWER DENSITY VERSUS RADIUS (CYLINDRICAL DIODE)

The temperature profile computed via equations (1) and (2) can be used to determine the current and power distributions, denoted respectively as J(r) and P(r), by an iterative procedure as outlined by Olsom[3], but modified to include the radial dependancy of the temperature and current densities. The analytical relations used in the iterative computational procedure are as follows:

(i) The saturation current density $J_s(r)$ versus peak electric field intensity, $\xi_m(r)$ at a temperature T(r):

$$J_s(r) = A^{**} T^2(r) \exp\left[\frac{-(\phi_B - \sqrt{(q\xi_m(r)/4\pi\epsilon}}{k\frac{T(r)}{q}}\right] \quad (3)$$

where A^{**} is the Richardson constant, k is the Boltzmann Constant, ϕ_B is the Schottky-barrier height, q is the electronic charge and ϵ is the permittivity of the device-medium.

(ii) Avalanche multiplication factor:

$$M(r) = J(r)/J_s(r) \quad (4)$$

where J(r) is the local current density.

(iii) Avalanche multiplication factor versus impact ionization coefficient, $\alpha(r)$:

$$1 - \frac{1}{M(r)} = \int_0^{W(r)} \alpha(r)\, dr \quad (5)$$

where $\alpha(r) = a(r) \exp\left[-[b(r)/\xi_m(r)]^2\right]$.

Further, a(r) and b(r) are temperature dependent ionization constants[13] and W(r) is the local extension of depletion region. It is related to $\xi_m(r)$ and carrier space change effects via Gauss law as given below:

$$W(r) = \xi_m(r)/[qN_D - J(r)/v_d(r)] \quad (6)$$

where N_D is the doping level and $v_d^{(v)}$ is the local electron drift velocity.

(iv) Lastly, the local current density can be expressed via space charge resistance concept as follows:

$$J(r) = \left[qN_D - \frac{\epsilon\xi_m^2(r)}{2V}\right] v_d(r) \quad (7)$$

where V is the applied diode voltage.

Hence, the power density P(r) is given by

$$P(r) = J(r) \times V \quad (8)$$

A typical power density variation with respect to r is shown in Figure 2b. In the computational procedure, this nonuniform profile of P(r) is approximated by the superposition of a series of constant power density profiles. Corresponding to P_{min} in Figure 2b, the temperature profile is obtained via equations (1 and 2). And the effect of each incremental (uniform) power densities ΔP is determined by superposing the temperature distribution due to a dissipation ΔP over a disk radius R and the one which would result from a fictitious dissipation of -ΔP over a disk radius of a, again by using equations (1 and 2). Once the new temperature T(r) is obtained, the procedure is iterated till the temperature profiles at two consecutive iterations do not differ from each other by more than a permissible error. Hence, from the final solution for J(r), the diode current is calculated by integrating the current density profile over the diode area.

Annular-Ring Mesa Diode

The treatment of annular ring diodes (Figure 1b) is similar to that of the cylindrical diode. That is, initially a uniform power density dissipation (P) is presumed over a disk of radius R_2 which is superimposed with a uniform power density (-P) "dissipated" over a disk radius of R_1 (Figure 1b). The resulting temperature profile is schematically shown in Figure 3a

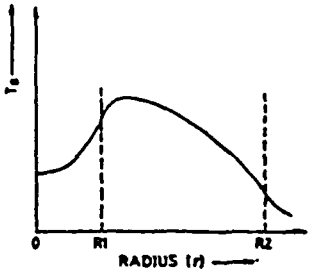


FIG. 3(a) TEMPERATURE PROFILE AT THE TOP SURFACE OF THE HEAT SINK (ANNULAR RING DIODE)

The maximum temperature occurs within the diode at a point relatively close to the inner edge of the annular ring. Figure 3b depicts the power density profile associated with such a temperature distribution. The discrete approximation of the power density profile by superposing quantized, constant-density levels (ΔP) required for iterative computation, is also illustrated in Figure 3b.

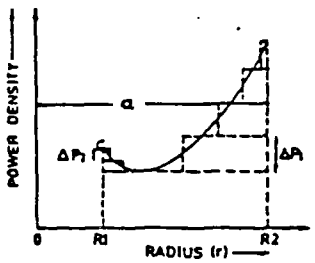


FIG. 3(b) POWER DENSITY VERSUS RADIUS (ANNULAR RING DIODE)

Pulsed Operation

Under pulsed conditions, the temperature and current density profiles are computed as follows: As IMPATTs operate at large duty cycles (above 10%) and as the diode/heat-sink thermal time-constant is much larger than the pulse-duration, the temperature at a given point is estimated by superposing a time average value $\bar{T}(r)$ with a transient increment $\Delta T(r,\tau) = 2P(r,t)\sqrt{\alpha t}/k\pi^{1/2}$, where α is the diode/heat-sink thermal diffusivity and P(r,t) is the instantaneous local power density. This time-dependent temperature distri-

bution is then used to compute the instantaneous current-density profile in the same manner as in the CW operation.

Results and Discussion

A. Failure Mechanisms

To analyze the mechanism(s) of failure, three versions of diode structures, namely single mesa, quad-mesa[17] and annular-ring mesa[13] mounted on copper or diamond heat-sink are considered for relevant computer simulation. All the structures are assumed to have an effective cross-sectional area A equal to $5.6 \times 10^{-4} cm^2$. The annular ring mesa structure with outer-to-inner radius ratio of R_2/R_1, has the same circumference as the quad-mesa diode. The semiconductor is assumed to be doped n-GaAs with a doping level of N_D equal to 10^{-16} cm^{-3}. For the n-GaAs-to-refractory metal (Pt, Wo etc.) contact the Schottky-barrier height ϕ_B is typically 0.8ev which is used in the computations.

The computed d.c. J-V characterisitics of test diodes (mounted on Cu heat-sinks) are presented in Figures 4a-6a. These illustrations display the average current density $\bar{J} = I/A$, the current density at the core of the cylindrical diodes (J_c) and the edge current density, J_E, as functions of the applied diode voltage, V. For the annular structures, the outer and inner current densities are denoted as J_{E1} and J_{E2}, respectively. The current density at the hottest zone of the annular diode is depicted as J_H. In the computations, the thermal resistance associated with the contacts and plating metallic layers is ignored.

Figures 4b-6b illustrate the radial variation of the current density and the temperature at the diode/heat-sink interface, for maximum approximate temperatures of 250°C and 350°C. The corresponding d.c. bias conditions are also indicated. In the case of annular structures, the temperature profile along the entire heat-sink surface is shown on appropriate diagrams.

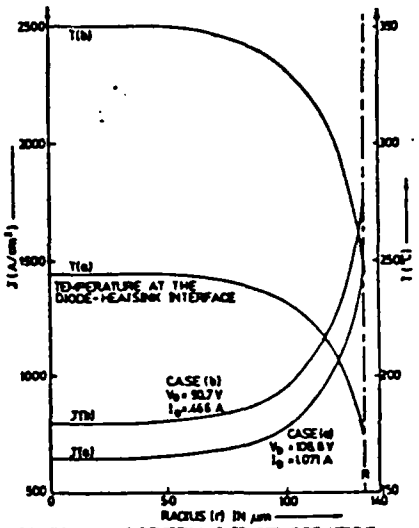


FIG. 4(b) CURRENT DENSITY AND TEMPERATURE VERSUS RADIUS (SINGLE MESA IMPATT ON COPPER HEAT SINK)

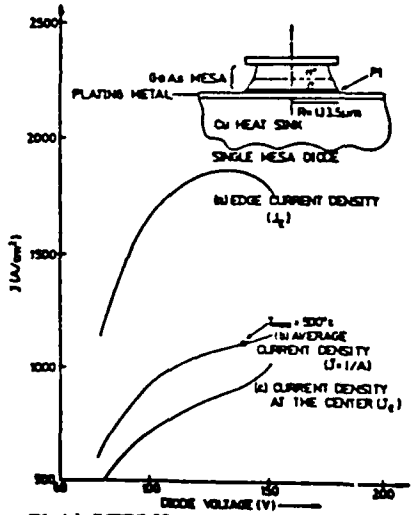


FIG. 4(a) CURRENT DENSITY VERSUS DIODE VOLTAGE (SINGLE MESA IMPATT ON Cu HEAT SINK)

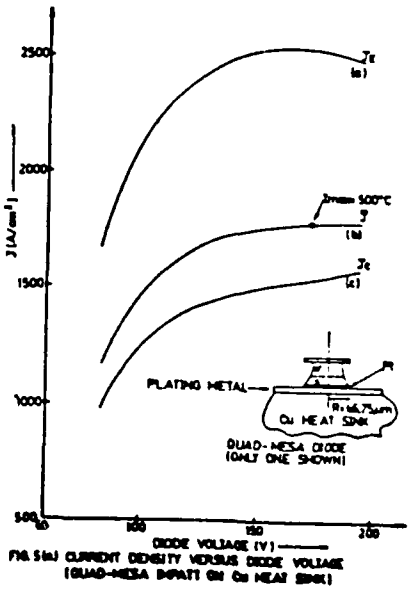
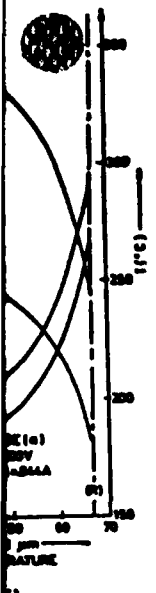


FIG. 5(a) CURRENT DENSITY VERSUS DIODE VOLTAGE (QUAD-MESA IMPATT ON Cu HEAT SINK)



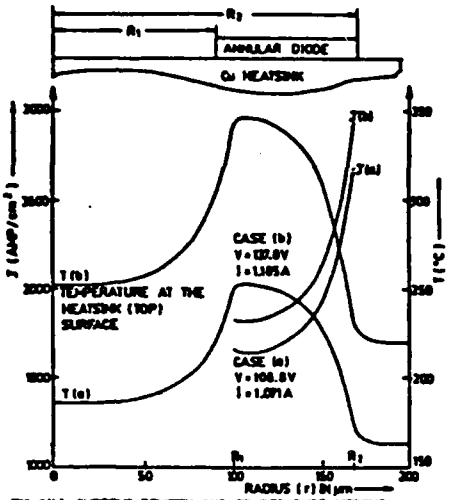
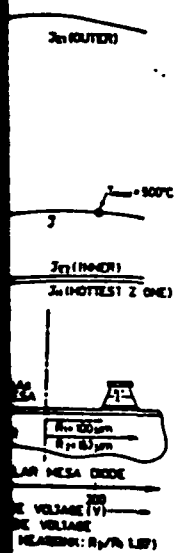


FIG. 6(b) CURRENT DENSITY AND TEMPERATURE VERSUS RADIUS (ANNULAR RING DIODE ON Cu HEATSINK R_2/R_1 = 1.67)



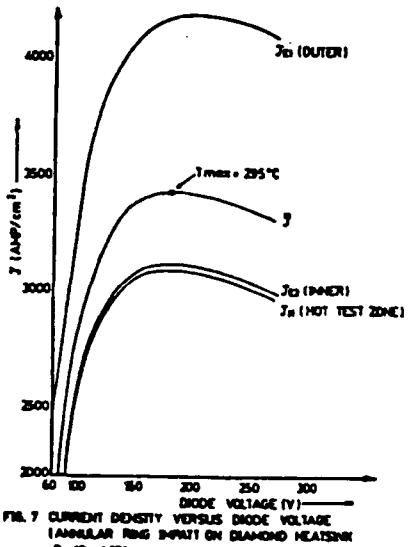


FIG. 7 CURRENT DENSITY VERSUS DIODE VOLTAGE (ANNULAR RING IMPATT ON DIAMOND HEATSINK R_2/R_1 = 1.67)

sing PDR region. At these temperatures, . current flow due to thermally generated n the depletion layer is several hundreds ince, the corresponding increase in the tion would naturally result in a thermal

ng the IMPATTs which are fabricated thermal designs, the failure mechanism ally initiated. These diodes have a arrying capability as shown on Figures 6a example, the diode in Figure 7 has a sink, and if its bias current is kept k level, the computed maximum function s less than 350°C. Also, the current ie warmest part of the diode does not reasing PDR. All these conditions are safe operation of the diode. However, in bias current in excess of the peak astrophic; and in an attempt to allow current flow, the diode voltage and er dissipation would reach unacceptable he edge regions suffering to a maximum ch as they carry the largest current ctually, the diode would burnout before ble operating point. Hence, for reliable e bias current should be limited to the peak level, by a margin of safety.

y of Various Diode Designs: A Comparison

a better heat-sink in general has [6,17] to be the most important aspect he power handling capability of IMPATTs. pose, diamond heat-sinks are normally

r heat-sinks (as well as with diamond), mall area diodes or realizing annular also would provide improved performance the present analysis.

presents the relative power handling f the best diodes studied in the present . It refers to CW operation with safe tion temperature of 250°C. The results ond heat-sink improves the power handling a factor of 2.5 over copper; and annular s show an improvement of about 25% mesa devices while retaining comparable formity in current distribution which le factor concerning the efficiency, g sensitivity of IMPATT diodes.

Under Pulsed Operation:

ty cycle of 10% and peak power levels as those resulting in a maximum junction f 250°C under CW operation, the how that the IMPATTs are relatively tance, the core temperature of quad-mesa mond heat-sink is only 45°C when they peak power level of 410 W. However, iode temperature being very low, the ion becomes intense resulting in current large as 5800 A/cm^2 in the cooler, gions. Such high current densities iode failure by forcing it to operate region with the current distribution able across the diode. The current will be the highest at the locales irrent density. It means that under s, the catastrophic high density sheath e mesa edge is rather inevitable.

Table 1. Comparison of the Power Handling Capabilities of Different GaAs Schottky-barrier IMPATT diodes (Maximum Function Temperature = 250°C)
CW Operation

No.	Design Type	Diode Voltage and Current	D.C. Input Power*	Relative Power Handling Capacity
1	Single-mesa on Cu Heat-Sink	V = 90.70 V I = 0.466 A	P = 42.3 W	1.00
2	Quad-mesa[17] on Cu Heat-sink	V = 103 V I = 0.844 A	P = 86.9 W	2.06
3	Annular-ring mesa[13] on Cu Heat-sink $R2/R_1$ = 100 μm/167 μm = 1.67	V = 108.8 V I = 1.071 A	P = 116.5 W	2.76
4	Single-mesa on Diamond Heat-sink	V = 105.8 V I = 0.983 A	P = 104 W	2.46
5	Quad-mesa[17] on Diamond Heat-sink	V = 130 V I = 1.552 A	P = 201.8 W	4.77
6	Annular-ring mesa[13] on Diamond Heat-sink $R2/R_1$ = 1.67	V = 151 V I = 1.893 A	P = 285.8 W	6.76
7	Annular-ring mesa[13] on Diamond Heat-sink $R2/R_1$ = 142.6 μm/50 μm = 2.85	V = 142 V I = 1.687 A	P = 239.5 W	5.67

*Thermal resistance due to contact and plating metallic layers at the heat-sink/diode interface is neglected. Typically, this additional resistance may bring down power handling by 30%.

Conclusions

1. A two-dimensional current distribution modeling is necessary for the realistic analysis of the power handling capabilities of IMPATTs.
2. Diodes with distinct thermal designs have different I-V characteristics.
3. Poor thermal designs exhibit a decreasing PDR region followed by a current controlled NDR with current filamentation at the hot-spot as the probable failure mechanism.
4. Diodes with better thermal design show a distinct maximum bias current capability. Forcing the bias current above this level would push the IMPATT into a voltage-controlled NDR and the resulting failure will be due to excessive diode voltage among the test diodes considered.
5. Annular-ring IMPATTs indicate relatively superior performance characteristics.
6. High temperature conditions may also provoke diode failures, due to excessive generation of intrinsic carriers.
7. Under pulsed operation, IMPATT reliability is jeopardized not by a high junction temperature, but rather by an excessive current flow causing a high-density current sheath at the mesa periphery.
8. Unlike simple PN junction diodes, IMPATTs warrant a comprehensive numerical modeling to assess the Wunsch-Bell limit of catastrophy due to thermal runaway.

Acknowledgements

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A possible mechanism of latent failure due to electrical overstressing in microelectronic devices is the time-dependent (cumulative) thermoelastic response of the device medium. That is, latent modes of failure can be attributed to the creeping of microflaws in the active locales of the device leading to deviatory performance characteristics. The thermoelastic response of the device is governed by both the thermodynamic inhomogeneities of the medium as well as by the pulsating/

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transient nature of the external stimuli. The present theoretical analysis on creep percolation can supplement the (latent mode) failure analysis based on micrographic studies of failed devices; hence the statistical prediction of latent failure time is possible with the data acquired via accelerated tests and calculations based on the equivalent aging principle.

FAILURES IN MICROELECTRONIC DEVICES

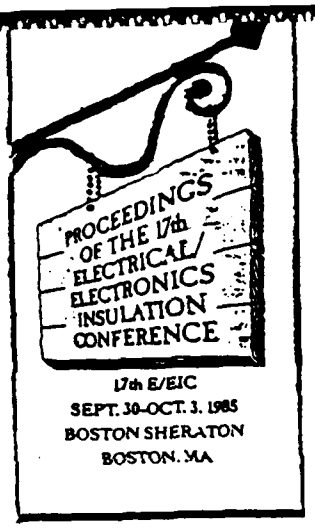
DUE TO THERMOELASTIC STRAINS

CAUSED BY ELECTRICAL OVERSTRESSINGS

a. Threat to Microelectronic Devices from Nonsinusoidal Repetitive EOS

b. Residual Fatigues in Microelectronic Devices Due to Repetitive EOS

c. Thermoelastic Strains in Microelectronic Strains: Creep Propagation



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ON THE THREAT TO DIELECTRIC-BASED ELECTRONIC DEVICES AND COMPONENTS FROM REPETITIVE NONSINUSOIDAL ELECTRICAL OVERSTRESSES —A REVIEW

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SUMMARY

Microelectronic devices and components are essentially dielectric-based monolithic structures with some additional metallization parts. These integrated circuits are highly susceptible to woundings arising from zappings due to electrical transients. Presently, electrostatic discharge(ESD)-based repetitive overstressings which may render the devices in a state of latent mode of failure are considered.[1] Such wounded or 'rogue' components may still be functional with deviatory characteristics, and are potentially prone to catastrophic failures on subsequent stress-repetitions.[2] The time-dependent degrading performance of wounded components is quantified via static-induced electrothermal effects in the device structure. The aging of the device is specified in terms of four possible damaging influences; namely, the elevated temperature, intensive electric field, depletory electromigration, and undue thermoelastic stresses. Based on the relative severity of these influences, a lethality endurance factor (L.E.F) is defined to estimate the failure time. Enhancement of severity due to pulsed waveform is also discussed. Lastly, the latent failure is regarded as the belated response due to slow endochronic growth of microfractures (creeping) caused by thermoelastic stresses arising from repetitive zappings.

INTRODUCTION

In the area of microelectronics there is an increased awareness to assess the long-term reliability of semiconductor devices which are susceptible to damages due to electrothermal effects at the dielectric and metallization interiors of the device arising from electrical overstresses caused by electrostatic discharges/transients.[2] High-intensity electrostatic zappings normally provocate catastrophic failures in the device either by burnouts due to high current densities or by dielectric puncturing (breakdown) resulting from high electric field intensities across capacitive elements.[2] For example, high-current burnouts are common at PN junctions and metallizations, and dielectric breakdowns have been observed at the thin gate-oxide layers of MOS structures. While high-intensity zaps would induce the aforesaid catastrophic failures, low-level transients may be regarded as the causative factors for the so-called 'soft' or latent type of failures in which the test devices exhibit endochronic performance degradation. Recurrence of zaps would ultimately lead the 'wounded' devices from the dormant stage of (mal)functionability to the out-of-spec or catastrophic condition.[1] The performance degradation or forced-aging due to electrical overstressing not only reduces the life expectancy of the device but also would necessitate costly field-repairs due to the unpredictable or 'phantamous' appearance of menacing latent failures.[1]

Presently the interaction of repetitive electrical transients and the device is studied to assess the extent of threat involved due to latent failures by formulating a quantitative description of the performance degradation or forced acceleration of the aging process.

ENDOCHRONIC MODEL

Latent failure occurs when a device takes multiple (low-level) zaps at random (or regular) intervals and the resulting wounding remains dormant over an unspecified period with the complete out-of-spec condition showing up at a much later time. The time dependent or endochronic performance degradation of the device and the belated failure can be expressed by a constitutive law, in terms of a generic function S(t) as follows:[3]

$$S(t) = S_i \exp[-a/T^*(t)] \cdot [\xi(t)/\xi_i]^{-\ell+b/T^*(t)} \cdot [C(t)/C_i]^{-m+c/T^*(t)} \cdot [M(t)/M_i]^{-n+d/T^*(t)} \quad (1)$$

where a, b, c, d are constants and $T^*(t)$ is a time-dependent temperature function given by $T^*(t) = T_i\, T(t)/T(t)+T_i$. Here T_i denotes the initial temperature and T(t) is the hot-spot temperature within the device at an observation time, t. Further, in Equation (1) S_i depicts the initial value of the generic parameter S and the exponential term represents the thermal life of the device as governed by the Arrhenius model. The quantities ξ, C, and M are time-dependent electrical, chemical, and mechanical stress parameters respectively and the initial values of ξ, C, and M are ξ_i, C_i, and M_i (respectively), below which the corresponding processes of aging are insignificant. The terms containing ξ, C, and M in Equation (1) follow the inverse power law depicting endochronic deteriorations and the quantities ℓ, m, and n denote respectively the electrical, chemical, and mechanical endurance coefficients characterizing respective aging processes.

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Equation (1) essentially depicts four major failure-inducing mechanisms. The domination of one particular process would depend on the strength of the excitation source (namely the ESD) and the infrastructure of the device. For example, intense transients can melt the PN junctions and/or metallizations; the resulting damage can therefore be regarded primarily as thermal. Likewise, dielectric-breakdowns at the gate-oxides of MOS structures are failures due to high electrical field stressing (ξ). Further, electromigration of metals at vulnerable zones, inducing localized pittings and voids, is a thermochemical/diffusion-based failure governed by the factor C. Mechanical damage characterized by the quantity M would often result from thermoelastic stresses which may develop in the composite-device structure due to thermal gradients and other thermodynamical inhomogeneties.[4]

Both the current-induced burnouts (melting) and voltage-induced dielectric breakdowns are, in general, catastrophic in nature, and therefore the relevant causative parameters are considered to be of the highest severity. With low level zaps, however, the degradation (say due to electromigration or thermoelectric straining) would be relatively less severe and the failure would take latent mode based on the cumulative growth of electromigration and/or thermoelastic microfracturing. Hence, representing the net failure process of Equation (1) by a monotonic decay function such as,

$$S(t) = S_i \exp(-K_o t) \tag{2}$$

(where K_o is the decay-rate constant), it is possible to specify the endurance of the device to lethality for different severity conditions, as follows:

$$\text{Lethality Endurance Factor (L.E.F)} = \frac{S(t)\,\text{Actual Process}}{S(t)\,\text{Catastrohic Process}} \tag{3}$$

Hence, for a catastrophic failure (either current induced or voltage induced), the severity actor (S.F) is taken as 1 and the corresponding L.E.F is equal to 1. However, for less severe dosages (S.F<1), the corresponding value of L.E.F can be written as,

$$\text{L.E.F}\Big|_{\text{S.F}<1} = \frac{K_1 [C(t)/C_i]^{-m+c/T^*(t)}}{S(t)\big|_{\text{Catastrophic Process}}}$$

$$= \frac{K_2 [M(t)/M_i)^{-n+d/T^*(t)}}{S(t)\big|_{\text{Catastrophic Process}}} \tag{4}$$

depending on the mechanism involved being electromigration or thermoelastic creeping, and K_1 and K_2 are constants of proportionality. The value of L.E.F in Equation (4) would be greater than 1, depicting the higher endurance by the device to zaps of lower intensity or severity. It can be shown that L.E.F is also identically equal to the ratio of failure times of the actual and catastrophic phenomena. That is,

$$\text{L.E.F} = \frac{(t_d)\big|_{\text{Actual Process}}}{(t_d)\big|_{\text{Catastrophic Process}}} \tag{5}$$

where t_d is the time-to-failure.

Explicit determination of L.E.F and S.F can be done by considering the characteristics of the ESD source and the static discharge path as described in the following section:

DETERMINATION OF L.E.F & S.F: ESD MODELS

The ESD phenomena normally encountered can be simulated by three well-established models; *namely*,[5] (i) human-body model, (ii) charged-device model, and (iii) field-induced model. The human-body model (Fig. 1) depicts the transfer of static from a charged individual to ground via the test device. Charged-device model represents the bleed-off of accumulated charge upon the device-surface to ground through the pin and conductive parts of the active device (Fig. 2). The third model simulates the effect of the charge distribution and discharge, when a device is exposed to a static-electric field (Fig. 3).

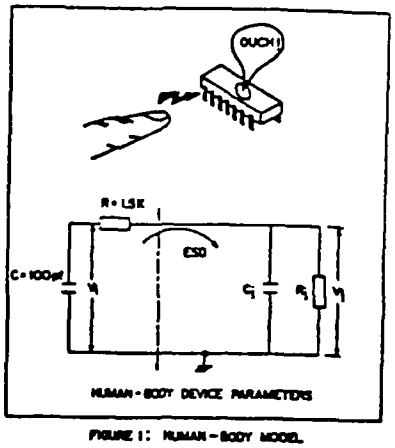


FIGURE 1: HUMAN-BODY MODEL

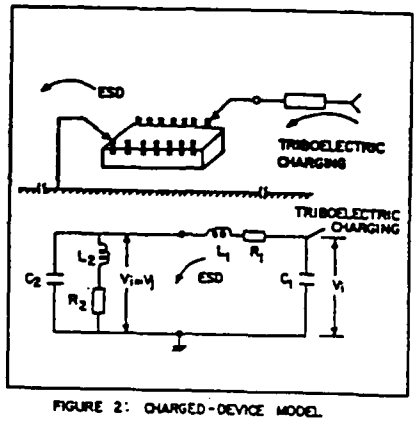


FIGURE 2: CHARGED-DEVICE MODEL

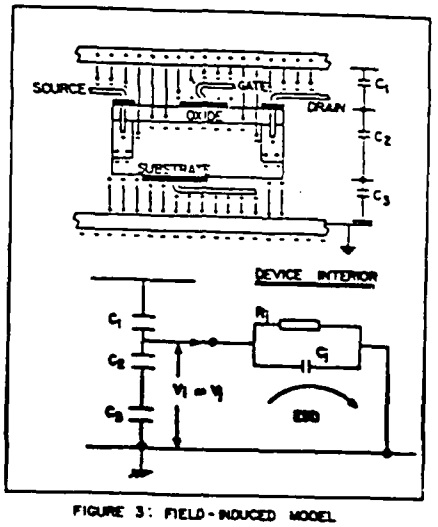


FIGURE 3: FIELD-INDUCED MODEL

The severity of zapping in each model is determined by the source voltage (V_i) and the load conditions of the discharge path. The corresponding lethality can be assessed by computing the average junction dissipation per unit area (if the lethality is current-based) given by,

$$P_d(t) = \frac{1}{At} \int_0^t [V_j^2(t)/R_j]dt \qquad (6)$$

where A is the junction area. Further, a complete or catastrophic failure would occur when the junction melts and the corresponding power density $P_c(t)$ can be calculated from the so-called Wunsch-Bell model.[6] It is given by,

$$P_c(t) = \sqrt{\pi k \rho C_p}\,(T_m - T_i)\,t^{-\frac{1}{2}} \qquad (7)$$

where k, ρ, and C_p are respectively the thermal conductivity, density, and heat capacity of the device material with a melting point equal to T_m. Hence, the lethality endurance factor (L.E.F) is given by,

$$L.E.F = \frac{\tau_1}{\tau_2} \qquad (8)$$

where τ_1 is determined by the equation $P_d(\tau_1) = P_c(\tau_1)$; and τ_2 is the catastrophic failure-time determined by the Wunsch-Bell relation (applied to spherical hot-spot), and is nearly equal to ($A \rho C_p/35k$).

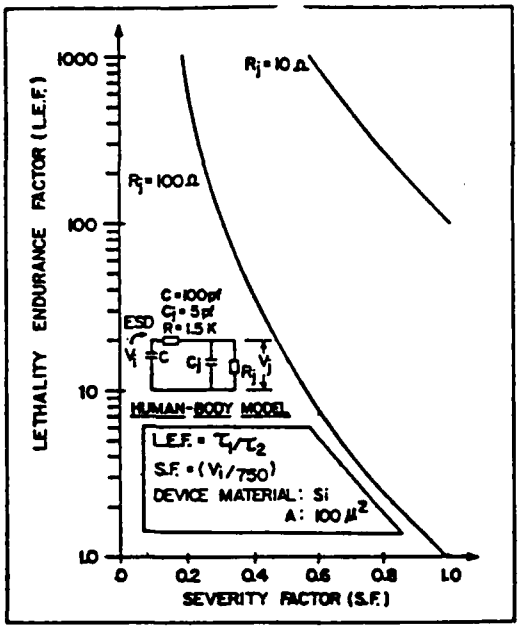


FIGURE 4 : LETHALITY CHARACTERISTICS OF CURRENT-BASED FAILURE

For the human-body model shown in Figure 1, by taking the severity factor (S.F) as 1 corresponding to V_i = 750V, the computed S.F versus L.E.F is shown in Figure 4. For different component values of the simulated charged-device circuit (Fig. 2), the calculated values of L.E.F are listed in Table 1. These results indicate the dependency of lethality on source as well as loading conditions.

The extent of severity would also depend on the wave-shape and rate of occurrence of the transients. Such enhanced severity can be quantified by a risk-coefficient γ representing the overvoltage effects of recurring transients. It is given by:

$$\gamma = \frac{(1+\tan^2\delta)\omega^2}{2\pi^2} \sum_1^{\infty} \frac{n^2 |F(n\omega)|^2}{1+n^2\tan^2\delta} \qquad (9)$$

where $\omega = 2\pi/T$ and T is the pulse repetition rate (or average number of zero-crossings if the occurrence is random), u is the pulsating component of the transient and F is the Fourier transform of the exciting time function. Further, the quantity tan δ denotes the loss-tangent of the device-dielectric at the angular frequency of ω. The risk-coefficient γ in general would be larger in comparison to unity (depicting increased

Table 1: Calculated Lethality for the Charged-Device Model (Figure 2)

V_i = 500V; Material: Si; A = 100 μm^2

L_1 = 10nH; C_1 = 3 pF; R_1 = 1Ω

No.	Case	L_2 nH	C_2 pF	t_d (Wunsch-Bell) ns	t_d (Actual) ns	L.E.F
1.	Worst Case A: Low L_2, Low C_2	10	1		0.1	0.003
2.	Worst Case B: Low L_2, Med C_2	10	1		0.3	0.009
3.	Expected Case A: Med L_2, Low C_2	50	1	33	0.5	0.015
4.	Expected Case B: Med L_2, Med C_2	50	10		9.0	0.273
5.	High Inductance Discharge Path: High L_2, Low C_2	100	1		6.0	0.182

power dissipation) when the transients are narrow (short-duration) pulses. Typical static-discharge waveforms are shown in Figure 5. For random recurrence of transients, the Fourier transform in Equation (9) can be obtained from the relevant autocorrelation calculations.

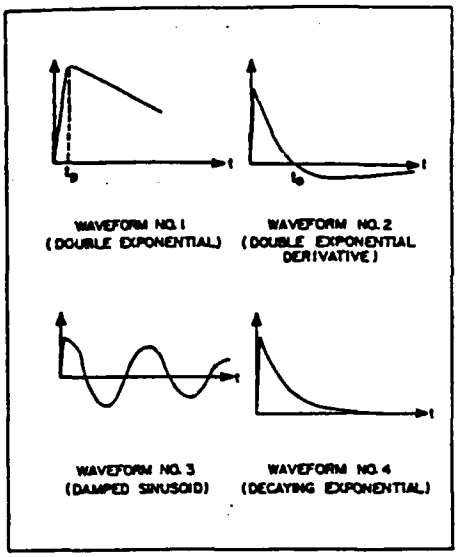


FIGURE 5: TYPICAL ELECTROSTATIC TRANSIENTS

When a voltage-based noncatastrophic failure (such as in a MOSFET) is considered, the performance degradation can be assessed from the enhanced nonlinearity of the CV characteristics. By measuring the distortion factor of the wounded device, it is possible to assess the severity and the lethality involved. Figure 6 illustrates a typical L.E.F versus S.F curve of a MOSFET, obtained by measuring the 3rd harmonic distortion in the transfer characteristics of a stressed device.

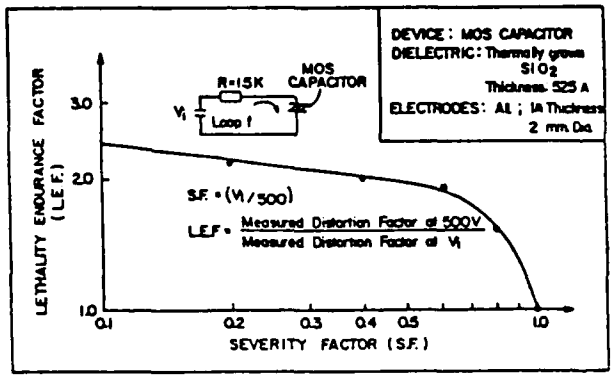


FIGURE 6: LETHALITY CHARACTERISTICS OF VOLTAGE-BASED FAILURE

LATENT FAILURE

As mentioned before, when less severe but repeated stressing prevails, slow material depletion/damage could occur and it would cumulatively build up leading to a belated out-of-spec or irreversible damage condition. In such latent failures, the material damage is often regarded as due to metal (Al, Au, etc.) migration from crucial sites causing line-to-line short circuits or interconnection ruptures (open-circuits). Such electromigration is essentially a thermochemical process governed by the factor C of Equation (1).

Presently, another possibility of microrupture is considered. That is, owing to the existence of thermodynamic inhomogenities in the device structure, the electrothermal processes due to zappings can possibly induce thermoelastic stresses within the composite dielectric interiors of the device. The corresponding strains/creeps can cumulatively build up (or propogate) by receiving repeated zaps, ultimately reaching an active site, leading to a failure. When an ESD sets up a temperature gradient of ΔT at a hot-spot inside the device, the maximum thermoelastic stress that would develop is given by

$$\sigma_{max} = \frac{\alpha(T) E \Delta T}{1-\nu} \qquad (10)$$

where α and E are the coefficient of thermal expansion and Young's modulus of elasticity of the device material respectively; and ν denotes the Poisson's ratio. In Figure 7, considering S_1 as the device material, σ_{max} is plotted as a function of temperature, T. Also shown in Figure 7 is the variation of fracture stress with respect to the temperature.[7] It could be evinced from Figure 7 that the thermoelastic stress could exceed the fracture strength of the material even at a temperature much below the melting point or the Wunsch-Bell's limit of catastrophy.[8] Hence, at low severity factors (for which the temperature elevation is well below the melting point), the lethality endurance is possibly limited by cumulative effects of thermoelastic rupturing and thermal shocks due to repeated stressings which would eventually lead to the observed latent failures.

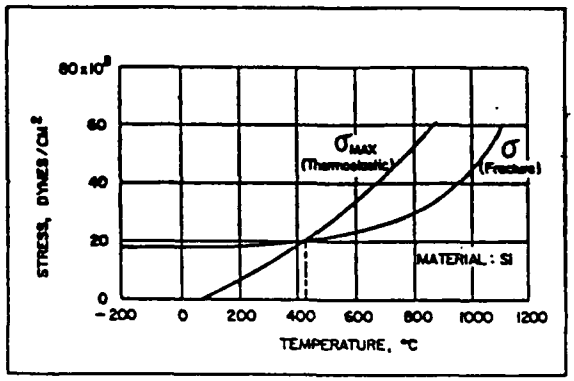


FIGURE 7: THERMOELASTIC AND FRACTURE STRESS VERSUS TEMPERATURE

Work is in progress to determine the average number of zaps per unit time required to cause a latent failure. This would enable the prediction of latent-failure time. Further, a systematic accelerated aging procedure and an algorithm based on the principle of equivalent aging are being developed to assess the statistics of latent failures, pertaining to microelectronic devices. The aging would be assessed by deviatoric leakage current and/or nonlinear transfer characteristics of the device.

CONCLUSIONS

A possible mechanism of latent failure due to ESDs in microelectronic devices is the time-dependent (cumulative) thermoelastic response of the device medium. Latent mode of failures can be assessed via two quantifiable terms; namely, severity factor (S.F) depicting the extant of causative influance and

lethality endurance factor (L.E.F) denoting the degree of deleterious effects observed. Both S.F and L.E.F are governed by the source (ESD) and load (discharge path, device) conditions.

ACKNOWLEDGEMENT

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RESIDUAL FATIGUES IN MICROELECTRONIC DEVICES DUE TO THERMOELASTIC STRAINS CAUSED BY REPETITIVE ELECTRICAL OVERSTRESSINGS: A MODEL FOR LATENT FAILURES

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Summary

Latent ESD/EOS effects produce no detectable changes in device performance at the time of ESD/EOS event(s), but subsequently produce deviatory device characteristics during normal use. The causative factors and the mechanism(s) of EOS-based latent failures are subtle in nature. However, considering the time-dependent degradation observed at low or subcatastrophic thresholds of static-exposure, the latent failure induction can be attributed to the cumulative buildup of strains due to thermoelastic stresses caused by repetitive zaps. Presently, the interaction between repetitive transients and the device is specified by two quantifiable terms designated as severity factor (SF) and lethality endurance factor (LEF). A thermodynamical analysis is developed to portray the thermoelastic straining, and the resulting endochronic response of stress-relief is studied by a constitutive modeling of the creep involved.

Introduction

In the area of microelectronics there is an increased awareness to assess the long-term reliability of semiconductor devices which are susceptible to damages due to electrothermal effects at the dielectric and metallization interiors of the device arising from electrical overstresses caused by electrostatic discharges/transients. High intensity electrostatic zappings normally provocate catastrophic failures in the device either by burnouts due to high current densities or by dielectric puncturing (breakdown) resulting from high electric field intensities across capacitive elements (Fig. 1). For example, high-current burnouts are common at PN junctions and metallizations, and dielectric breakdowns have been observed at the thin gate-oxide layers of MOS structures. While high-intensity zaps would induce the aforesaid catastrophic failures, low-level transients may be regarded as the causative factors for the so-called 'soft' or latent type of failures in which the test devices exhibit endochronic performance degradation. Recurrence of zaps would ultimately lead the 'wounded' devices from the dormant stage of (mal)functionability to the out-of-spec or catastrophic condition. The performance degradation or forced-aging due to electrical overstressing not only reduces the life expectancy of the device but also would necessitate costly field-repairs due to the unpredictable or 'phantasmous' appearance of menacing latent failures.[1]

The latent mode of device failure is expected to arise from the degradation of any generic property of the device under repeated electrical stressing. When the EOS is not large enough to cause a total or catastrophic failure, it may still be sufficient to wound the device through elastic stress formation. The wounded device may remain dormant over an (unspecified) period, but eventually, when it continues to receive repetitive zaps, the damage resulting from elastic stress becomes cumulative and turns the device into a rogue component with high chances of exhibiting malfunctions. Presently, a thermodynamical model is developed to depict the existence of thermoelastic stresses/strains arising from EOS-based electrothermal processes, and the interaction of repetitive transients with the device is studied to assess the extent of threat involved due to latent failure by formulating a quantitative description of the performance degradation or forced acceleration of the aging processes as governed by the elastic creep.

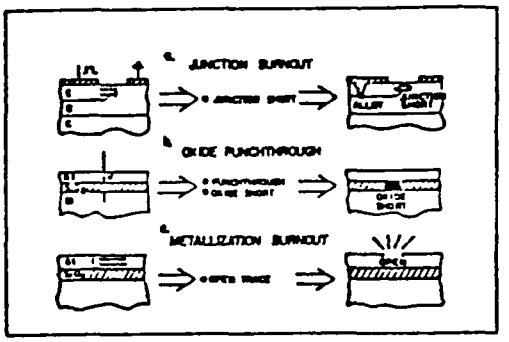


FIGURE 1: ESD/EOS BASED FAILURES

EOS-Induced Thermoelastic Effects: A Thermodynamical Formulation

External electrical overstressings would generate heat within the device due to I^2R loss and would set up a temperature gradient across the heterogeneous device media. Owing to the discontinuities (spatial or temporal) in the thermodynamical variables, namely, mass density (ρ), specific heats (C_p and C_v), thermal coefficient of expansion (α) and isothermal compressibility (K_T), or, due to inhomogeneous energy absorption characteristics, thermoelastic strains may be induced in the device which may initiate microcracks. Subsequent zaps would cause the percolation of the flaws to crucial sites (in the active parts of the device) leading to performance degradation and/or total failure.

Considering an arbitrary hot-spot (Fig. 2), the system relations based on conservation of mass, conservation of energy, and thermodynamical equations of state can be written as follows:[1]

$$d_t \rho + \rho \nabla . \bar{v} = 0 \qquad (1a)$$

$$\rho d_t v_i + \delta_j \sigma_{ij} = 0 \qquad (1b)$$

$$\sigma_{ij} \delta_j v_i + \rho d_t E_I = \rho W \qquad (1c)$$

$$d_t E_I = [-(C_p/\rho\alpha) + (1/\rho^2) \sigma_{ij} \delta_j v_i/\nabla.\bar{v}] d_t \rho + (C_v/\alpha) (k_T)_{ij} d_t \sigma_{ij} \qquad (1d)$$

where the operator d_t is the convective derivative equal to $\partial/\partial t + \bar{v}.\nabla$ where $\bar{v}$ is the bulk velocity of

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Table 1: Calculated Lethality for the Charged-Device Model (Fig. 4)

V_1 = 500V; Material: Si; A = 100 μm^2

L_1 = 10nH; C_1 = 3 pF; R_1 = 1Ω

No.	Case		L_2 nH	C_2 pF	t_d (Wunsch-Bell) ns	t_d (Actual) ns	LEF
1.	Worst Case A:	Low L_2 Low C_2	10	1		0.1	0.003
2.	Worst Case B:	Low L_2 Med C_2	10	1		0.3	0.009
3.	Expected Case A:	Med L_2 Low C_2	50	1	33	0.5	0.015
4.	Expected Case B:	Med L_2 Med C_2	50	10		9.0	0.273
5.	High Inductance Discharge Path:	High L_2	100	1		6.0	0.182

lethality endurance factor (LEF) is given by,

$$LEF = \frac{\tau_1}{\tau_2} \qquad (12)$$

where τ_1 is determined by the equation $P_d(\tau_1) = P_c(\tau_1)$; and τ_2 is the catastrophic failure-time determined by the Wunsch-Bell relation (applied to spherical hot-spot), and is nearly equal to $(A \rho C_p/35k)$.

For the human-body model shown in Fig. 3, by taking the severity factor (SF) as 1 corresponding to V_1 = 750V, the computed SF versus LEF is shown in Fig. 6. For different component values of the simulated charged-device circuit (Fig. 4), the calculated values of LEF are listed in Table 1. These results indicate the dependency of lethality on source as well as loading conditions.

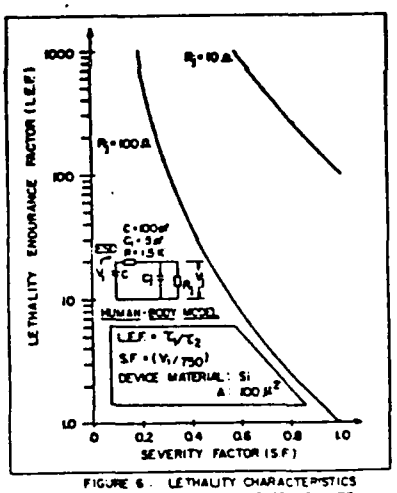


FIGURE 6. LETHALITY CHARACTERISTICS OF CURRENT-BASED FAILURE

When a voltage-based noncatastrophic failure (such as in a MOSFET) is considered, the performance degradation can be assessed from the enhanced nonlinearity of the CV characteristics. By measuring the distortion factor of the wounded device, it is possible to assess the severity and the lethality involved. Fig. 7 illustrates a typical LEF versus SF curve of a MOSFET, obtained by measuring the 3rd harmonic distortion in the transfer characteristics of a stressed device.[6]

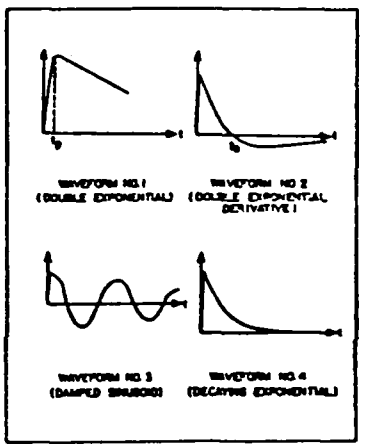


FIGURE 7. TYPICAL ELECTROSTATIC TRANSIENTS

The extent of severity would also depend on the wave-shape and rate of occurrence of the transients. Such enhanced severity can be quantified by a risk-coefficient γ representing the overvoltage effects of recurring transients. It is given by:

$$\gamma = \frac{(1+\tan^2\delta)\omega^2}{2\pi^2 u^2} \sum_{1}^{\infty} \frac{n^2 |F(n\omega)|^2}{1+n^2 \tan^2\delta} \qquad (13)$$

where $\omega = 2\pi/T$ and T is the pulse repetition rate (or average number of zero-crossings if the occurrence is random), u is the pulsating component of the transient and F is the Fourier transform of the exciting time function. Further, the quantity $\tan\delta$ denotes the loss-tangent of the device-dielectric at the angular frequency of ω. The risk-coefficient γ in general would be larger in comparison to unity (depicting increased power dissipation) when the transients are narrow (short-duration) pulses. Typical EOS waveforms are shown in Fig. 8. For random recurrence of

transients, the Fourier transform in equation (13) can be obtained from the relevant autocorrelation calculations.

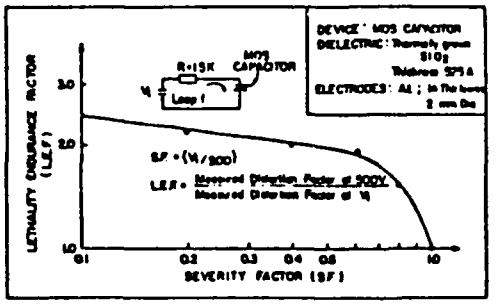


FIGURE 8 : LETHALITY CHARACTERISTICS OF VOLTAGE-BASED FAILURE

Thermoelastic Stressing

As mentioned before, when less severe but repeated stressing prevails, slow material depletion/damage could occur and it would cumulatively build up leading to a belated out-of-spec or irreversible damage condition. In such latent failures, the material damage is often regarded as due to metal (Al, Au, etc.) migration[7] from crucial sites causing line-to-line short circuits or interconnection ruptures (open-circuits). Such electromigration is essentially a thermochemical process governed by the factor C of equation (5).

Another possibility of microrupture, as indicated earlier, arises owing to the existence of thermodynamic inhomogenities in the device structure. That is, the electrothermal processes due to zappings can possibly induce thermoelastic stresses within the composite dielectric interiors of the device as specified by the thermodynamical relation of equation (3). The corresponding strains/creeps can cumulatively build up (or propogate) by receiving repeated zaps, ultimately reaching an active site, leading to a failure. When an ESD sets up a temperature gradient of ΔT at a hot-spot inside the device, the maximum thermoelastic stress that would develop is given by

$$\sigma_{max} = \frac{\alpha(T) E \Delta T}{1-\nu} \qquad (14)$$

where α and E are the coefficient of thermal expansion and Young's modulus of elasticity of the device material respectively; and ν denotes the Poisson's ratio. In Fig. 9, considering silicon and GaAs as the device materials, σ_{max} is plotted as a function of temperature, T. Also shown in Fig. 9 is the variation of fracture stress with respect the temperature. It could be evinced from Fig. 9 that the thermoelastic stress could exceed the fracture strength of the material even at a temperature much below the melting point or the Wunsch-Bell's limit of catastrophy. Hence, at low severity factors (for which the temperature elevation is well below the melting point), the lethality endurance is possibly limited by cumulative effects of thermoelastic rupturing and thermal shocks due to repeated stressings which would eventually lead to the observed latent failures.

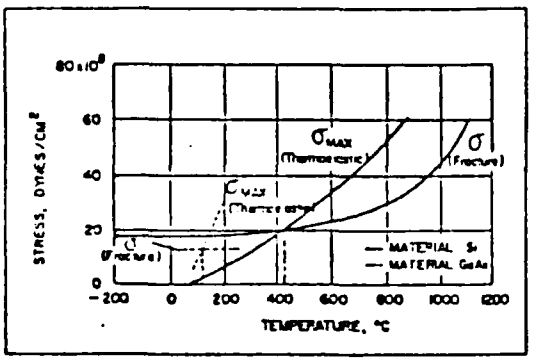


FIGURE 9 : THERMOELASTIC AND FRACTURE STRESS VERSUS TEMPERATURE

Percolation of Failure Front

Once a microflaw is initiated, subsequent external stimuli would encourage a cumulative growth of the deformation until a total failure occurs. Depending on the site of initiation (nucleation) of the microflaw, the extent of functional characteristics of the device been affected can be decided. As long as the initiation and growth of flaws are in the nonactive regions of the device, the catastrophic failure may not show up. Perhaps a performance degradation may occur. However, as the flaw percolates and reaches a vulnerable site or an active zone in the device, the device failure will be complete with an irreversible damage. Therefore, until the growth process culminates in a catastrophic or out-of-spec condition, a dormant state of failure would prevail. The propogation of a microflaw and the creep rupture of an electrically overstressed device can be studied by the following simple model:

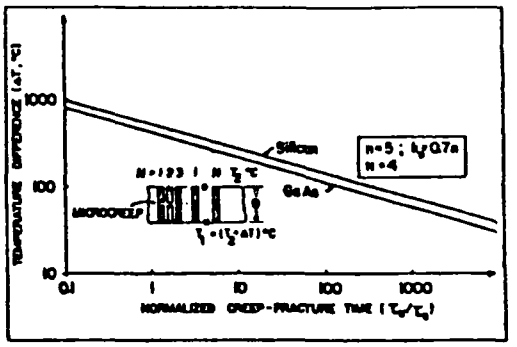


FIGURE 10: NORMALIZED CREEP FRACTURE TIME VS. DIFFERENTIAL TEMPERATURE

Consider a thin layer of the stressed materials of width B. Let T_1 and T_2 be temperatures at the two extremities of the layer as shown in Fig. 10, where $T_1 > T_2$. The test material being composite in nature, the analysis is done by dividing the layer into N-strips. Due to the temperature difference, the thermoelastic stress and strains at the i^{th} strip can be represented by the quantities σ_i and ϵ_i, respectively. If δ_i is the elongation of the i^{th} strip, then the basic equations of equilibrium are:

$$\sum_{i=1}^{N} \left(\frac{N+1-i}{N}\sigma_i\right) = \sum_{i=1}^{N} \epsilon_i \alpha_i \Delta T \equiv Q_A \qquad (15)$$

where ΔT is the temperature difference, (T_1-T_2). E_i and α_i are the Young's modulus and coefficient of thermal expansion of the i^{th} strip respectively.

The strain-displacement relation can be specified as

$$\epsilon_i = \delta_i / B, \qquad (16)$$

together with the compatibility condition,

$$\delta_i = \frac{N+1-i}{N}\delta_1 \quad . \qquad (17)$$

Further, the constitutive equations of creep initiation and growth are given by[6]

$$\epsilon_i = (\sigma_i/c_i) + \epsilon_c \tag{18a}$$

$$d\epsilon_c/dt = C_1 (\sigma_i/1-q_i)^{n_o} \tag{18b}$$

$$dq_i/dt = C_2 (\sigma_i/1-q_i)^{k_o} \tag{18c}$$

where C_1, C_2, n_o and k_o are material constants and ϵ_c is the creep-strain. The quantity q is a damage parameter which increases from zero in a virgin state to unity at rupture. For most of the materials the value[9] of n_o is less than 5 and k_o is nearly equal to 0.7 n_o.

When a continuous body occupying a volume V is acted upon the surface by a certain stress, the constitutive factor concerning steady creep behavior would be monotonic. That is, increases in stress would cause increases in the strain rate. For a steadily creeping material, the growth law of damage can be written as[6]

$$d\epsilon_c/dt = d\Omega_{k_o}/dt \tag{19}$$

and

$$dq/dt = C_2 \phi^{k_o}(\sigma) / (1-q)^{k_o} = \Omega_{k_o}(\sigma) / (1-q)^{k_o} \tag{20}$$

where $\Omega_{k_o}(\sigma) = C_1 \phi^{k_k}(\sigma)$ and $\phi(\sigma)$ is a scalar invariant of the stress function, σ.

Further, the specific rate of work done in the creep process or the strain-energy dissipation can be written as

$$\zeta(t) = \frac{1}{V}\iiint (1-q)^{k_o+1} dV. \tag{21}$$

Integrating the damage relation dq/dt of equation (20) over the volume of the body (V) and combining with equation (21), the following result is obtained:

$$(-1/k_o+1)\, d\zeta(t)/dt = \frac{1}{V}\iiint \Omega_{k_o}(\sigma)\, dV \quad . \tag{22}$$

The growth damage as decided by the above relation would culminate at a critical stress level of statically admissable value and then the rupture will take place. Initially, $q = 0$ throughout the body; that is, $\zeta(0) = 0$. At final rupture, $t = \tau_U$, $\zeta = \zeta_U > 0$. Hence by integrating equation (22) over the time interval $(0, \tau_U)$, the upper bound on life-time is obtained as,

$$\tau_U < V(1-\zeta_U) / [(1+k_o)\iiint C_1 \phi^{k_o}(\sigma)\, dV] \quad . \tag{23}$$

The steady-state stress for the multiple strip structure (Fig. 10) is given by[6]

$$\sigma_i = [(N+1-i)/N]^{1/n_o} Q_A / I_{n_o}(N), \quad i = 1,2,3... \tag{24}$$

where

$$I_o(N) = \sum_{i=1}^{N} [N+1-i/N]^{1+1/n_o}.$$

The corresponding upper bound of normalized rupture time can be estimated as:

$$\tau_U/\tau_o = F_U(k_o) / (\sigma/\sigma_o)^{k_o} \tag{25}$$

where τ_o is the rupture time of a single strip under the tensile stress σ_o and $\sigma = \alpha E \Delta T$; further,

$$F_U(k_o) = N\left\{\sum_{i=1}^{N} [(N+1-i)/N]^{k_o/k_o-1}\right\}^{k_o-1} \tag{26}$$

The variation of normalized creep-failure time as a function of temperature difference for a typical deteriorating semiconductor structure (thin layer) is shown in Fig. 10. Silicon and GaAs are taken as the test materials, and the failure is presumed to occur when the creep reaches the fourth strip (that is, $N = 4$).

In Fig. 10, a fast deterioration is indicated for large differential temperatures. That is, for higher severity levels, there is an accelerated damage percolation as expected. At subcatastrophic levels the failure percolation is belated and the failure involved would be of latent mode.

Conclusions

1. A possible mechanism of latent failures in microelectronic devices is the thermoelastic stress-relief cracks induced by repetitive electrostatic discharges at subcatastrophic levels.

2. The thermoelastic stressing is mainly governed by the thermodynamical discontinuities in the material variables and by the inhomogeneity of the source function.

3. The cause-effect relations involved in the ESD/EOS-based damages can be quantified via severity and lethality endurance factors (SF and LEF). The level of severity would specify the catastrophic and/or latent modes.

4. The extent of severity is also governed by the ESD source. That is, the severity factor (SF) and the corresponding lethality are determined by charge-transfer/discharge pertaining to human-body model, charge-device model, or field-induced model.

5. The endochronic response (damage) of the device is determined by the characteristics of the interacting pulsations, namely, repetition rate, shape, and amplitude.

6. The initiation and propagation of microcracks and flaws within the device are directly controlled by the extent of thermoelastic stressing.

7. The maximum thermoelastic stress can reach the fracture strength value at differential temperatures of magnitude well below the melting point. That is, structural damage can be anticipated at zap-levels considerably lower than the Wunsch-Bell limit of catastrophy.

8. For a specific device, on the basis of fault-isolation data gathered via micrographic studies on latent failed devices, the creep propagation can be traced and vulnerable zones prone to thermoelastic straining can be identified. In addition, data collected from parametric measurements under accelerated testing can be used to develop an algorithmic representation of creep-propagation and latent time-to-failure in terms of number of zaps per unit time. Relevant work is in progress.

Acknowledgement

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FAILURES IN MICROELECTRONIC DEVICES DUE TO THERMOELASTIC STRAINS CAUSED BY ELECTRICAL OVERSTRESSINGS

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ABSTRACT

The causative factors and mechanism(s) of latent-failures in microelectronic devices induced by electrical overstressing are subtle in nature. However, considering the age-dependent performance degradation that occurs at low thresholds of external electrical stressings (such as electrostatic discharge, electromagnetic pulsing, etc.) which may lead a device into out-of-spec conditions, the failure induction can be attributed to the cumulative buildup of residual strains within the device resulting from thermoelastic stresses caused by repetitive zaps. The corresponding thermal shock and fatigue can initiate microflaws in the device structure, and therefore the latent mode of device failure can be regarded as the endochronic response of the stress-relief in the device structure which can be analyzed by electromagnetics-based electrothermal/thermoelastic considerations as detailed in the present investigations.

INTRODUCTION

A major limitation that hangs over the future generation of microelectronic devices is the assurance of a suitable degree of reliability arising from physical considerations due to ultraminiaturization. Understanding the reliability attributes of monolithic integrated circuits requires knowledge of both physical and chemical phenomena that can occur after a device is manufactured and that can affect reliability [1]. In the course of development of complex, monolithic device structures, it has been observed that most failures could be characterized as function failures governed by electrical, thermal, chemical, and electrical-field factors. The related failure mechanisms expected to plague the devices can be grouped according to susceptible physical locales as indicated in Table 1.

The failure mechanisms can be further classified into two categories; namely, (i) persistent stressing due to temperature elevations caused by the operating current or due to environmental factors such as humidity which continuously act according to the Arrhenius process law, and, (ii) threshold-limited damage governed by a datum level of susceptibility of the device to the hazardous influence.

Table 1: Failure Mechanisms Expected to Affect Microelectronic Devices

Locales in the Device	Mechanism	Type of Failure
1. Conductors (Metallisations)	Stress Relief Cracks	Latent
	Electromigration	Latent
	Grain Size Effects	Latent
	Hillock Formation	Latent
	Corrosion	Latent
	Pitting	Catastrophic
2. Insulators (Dielectrics)	Stress Relief Cracks	Latent
	Surface Charge Accumulation	Latent
	Dielectric Breakdown	Catastrophic/Latent
	Charge Injection (Hot Carriers)	Catastrophic
3. Semiconductors	Defects/Imperfections	Catastrophic
	Oxygen Content	Latent
	Diffusion Faults	Catastrophic
4. Interfaces	Intermetallic Growths	Latent
	Adhesion Loss	Latent
	Contamination	Latent

While the stressings above the threshold level would cause irreversible (or catastrophic) damages, it is possible that low-level zaps can stimulate degradations in the device performance characteristics. A cumulative growth of performance degradation would eventually lead the device into out-of-spec conditions. This brand of failure is better known as the latent failure. Such time-dependent failures are often caused by low-level overstressings due to electrical transients or electrostatic discharges.

Presently, the endochronic performance degradation is analyzed as a thermoelastic-based creeping of microruptures arising from thermodynamical inhomogeneities in the composite device structure.

ENDOCHRONIC PERFORMANCE DEGRADATION

The time-dependent performance degradation of a microelectronic device and the belated failure can be modeled by a constitutive law in terms of a generic function S(t) given by [2]:

$$S(t) = S_i \exp\,[-a/T^*(t)]\;\; [\xi(t)/\xi_i]^{-\ell+b/T^*(t)}$$

$$[C(t)/C_i]^{-m+c/T^*(t)}\;\; [M(t)/M_i]^{-n+d/T^*(t)} \qquad (1)$$

where a,b,c,d are constants and $T^*(t)$ is a time-dependent temperature function given by $T^*(t) = T_i\, T(t)/[T(t) - T_i]$. Here, T_i denotes the initial temperature and T(t) is the hot-spot temperature within the device at an observation time, t. Further, in equation (1), S_i depicts the initial value of the generic parameter S and the exponential term represents the thermal life of the device as governed by the Arrhenius process. The quantities ξ, C, and M are time-dependent electrical, chemical, and mechanical stress parameters respectively; and their initial values are ξ_i, C_i, and M_i below which the corresponding processes of aging are insignificant. The terms containing ξ, C, and M in equation (1) follow the inverse power law depicting endochronic deteriorations; and the quantities ℓ, m, and n denote the corresponding electrical, mechanical, and chemical endurance coefficients respectively.

Equation (1) essentially represents four major failure-inducing mechanisms. The domination of one particular process would depend on the extent of the corresponding stress and the strength of endurance of the device infrastructure (to that particular stress). For example, intense electrical transients can melt PN junctions and/or metallizations; the resulting damage is therefore primarily thermal [3]. Likewise, dielectric breakdowns [4] at MOS-gate structures are failures due to high electric field stressing (ξ). Further, electromigration of metals (Al, Au, etc.) at vulnerable sites can induce localized or extended pittings and voids [5,6]. This is a thermochemical/diffusion-based failure which is governed by the factor C. Mechanical damage characterized by the quantity M would result from thermoelastic stresses which may develop in the composite device structure due to thermal gradients and other thermodynamical inhomogeneities as discussed below.

THERMOELASTIC STRESSES AND MICRODEFORMATIONS

External electrical overstressings would generate heat within the device due to I^2R loss, and would set up a temperature gradient across the heterogeneous device media. The spatial and/or temporal variables such as mass density (ρ), specific heats (C_p and C_v), thermal coefficient of expansion (α) and isothermal compressibility (k_T) would induce thermoelastic stresses which may initiate microcracks. Subsequent zaps would cause the creep-propogation and the percolation of cracks to crucial sites (such as metallization interconnections) would cause performance degradation and/or total failure.

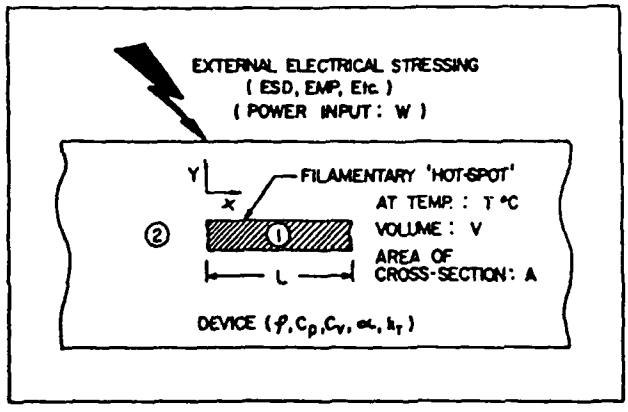


FIGURE 1: STRESSED DEVICE AND HOT-SPOT FORMATION

Considering an arbitrary hot-spot (Fig. 1), the system relations based on conservation of mass, conservation of energy, and thermodynamical equation of state can be written as follows [7]:

$$d_t\rho + \rho\nabla.\bar{v} = o \qquad (2a)$$

$$\rho d_t\, v_i + \delta_j\, \sigma_{ij} = o \qquad (2b)$$

$$\sigma_{ij}\, \delta_j\, v_i + \rho d_t\, E_I = \rho W \qquad (2c)$$

$$d_t\, E_I = \{-(C_p/\rho\alpha) + (1/\rho^2)\, \sigma_{ij}\, \delta_j\, v_i/\nabla.\bar{v}]\; d_t\rho$$

$$+ (C_v/\alpha)\; (k_T)_{ij}\; d_t\, \sigma_{ij} \qquad (2d)$$

where the operator d_t is the convective derivative equal to $\partial/\partial t + \bar{v}.\nabla$ where $\bar{v}$ is the bulk velocity of the thermoelastic vibration. Further, δ_j depicts the space derivative $\partial/\partial x_j$, and E_I is the internal (thermodynamic) energy density and W is the power input from the external stimulus. The quantity σ_{ij} represents the stress tensor.

A small hot-spot region (Fig. 1) can be regarded as mechanically isotropic and hence equations (2) can be simplified to obtain linear equations for $d_t\rho$, σ, and $\bar{v}$. They are given by [7]

$$\delta_t^2\, (\delta_t\rho) - C_o^2\, \nabla^2(\delta_t\rho) = [C_o^2\, \rho\alpha/C_p]_o\, \nabla^2 W \qquad (3a)$$

$$\delta_t^2\sigma - C_o^2\, \nabla^2\sigma = [\rho C_o^2\alpha\, /\, C_p]\, \delta_t\, W \qquad (3b)$$

$$\delta_t^2\, \bar{v} - C_o^2\nabla^2\bar{v} = -[C_o^2\alpha\, /\, C_p]\, \nabla W \qquad (3c)$$

where σ refers to the stress at time t in the homogeneous, isotropic hot-spot region, and C_o is the thermoelastic wave velocity in the device media. It is equal to $[(C_p/\rho C_v\, k_T)^{\frac{1}{2}}]_o$. (The suffix o denotes the equilibrium state and δ_t refers to the operator $\partial/\partial t$.)

The wave equations given by the relations (3) can be solved with appropriate boundary conditions if the hot-spot dimensions are specified. Thus, for a filamentary hot-spot of length L and cross-sectional area A (Fig. 1) which may result from a pulse input due to an external stressing (say, electrostatic discharge), the following solutions concerning the stress waves can be obtained [7]:

$$\sigma_{1,2}\,(x,t) = \sum_{n}^{\infty} A_{n_{1,2}}\, \frac{W(\omega_n)}{\omega_n}\, \exp\,(-j\omega_n t) \qquad (4)$$

where the indicies 1 and 2 represent the regions inside and outside the hot-spot; n is an odd integer, if $\tan\phi = (\rho C_o)_2/(\rho C_o)_1 < 1$; otherwise it is even. The coefficients A_{n_1} and A_{n_2} are given by,

$$A_{n_1} = (-1)^{\frac{n+1}{2}} \sqrt{2\pi}\, (\rho\alpha C_o^3/C_p L)_1\, [\cos\,(\omega_n\, x/C_{o_1})]$$

and

$$A_{n_2} = (-j)\, \sqrt{2\pi}\, (\rho\alpha C_o^3/2C_p L)_2\, \tan(2\phi)\, \exp[j\omega_n (x-L)/C_{o_2}] \qquad (5)$$

Further, $\omega_n = [(C_o)_1/2L]\,(n\pi - j\gamma_o)$ where γ_o is the solution of the equation $\coth(\gamma_o) + (-1)^n \operatorname{csch}(\gamma_o) = \tan\phi$.

For each frequency component ω_n the corresponding stress amplitude exhibits some resonance phenomena according to the value of the pulse width. The influence of pulse widths of electrical transients in causing performance degradation has been established via experimental studies [8,9] and the present analysis indicates the existence of elastic (resonant) stress waves arising from external stimuli which could possibly induce microdeformations.

The maximum stress developed at a vulnerable site due to a temperature gradient of ΔT is given by

$$\sigma_{max} = \alpha(T)\, E\, \Delta T\, /(1-\nu) \qquad (6)$$

where E is the Young's modulus of elasticity and ν is the Poisson's ratio. Considering silicon as the device material, σ_{max} is plotted in Fig. 2 as a function of T along with the variation of fracture strength with respect to temperature. It can be seen from Fig. 2 that the thermoelastic stress can exceed the fracture strength at a temperature well below the melting point (1215°C), indicating that even low-level zaps can possibly initiate microdeformations in the device via induction of thermoelastic stresses.

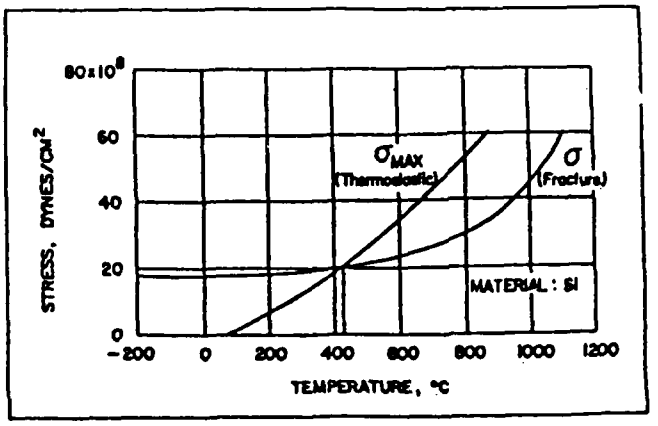


FIGURE 2: THERMOELASTIC AND FRACTURE STRESS VERSUS TEMPERATURE

PERCOLATION OF FAILURE-FRONT

Once a microflaw is initiated, subsequent external stimuli would encourage a cumulative growth of the deformation until a total failure occurs. Depending on the site of initiation of the microflaw, the extent to which the functional characteristics of the device are affected can be determined. As long as the initiation and growth of flaws are in the nonactive regions of the device, the catastrophic failure may not show up. Perhaps a performance degradation may occur. However, as the flaw percolates and reaches a vulnerable site or an active zone of the device, the device failure will be complete with an irreversible damage. Therefore, until the growth process culminates in a catastrophic or out-of-spec condition, a dormant state of failure would prevail. The propagation of a microflaw and the creep rupture of an electrically overstressed device can be studied by the following simple model:

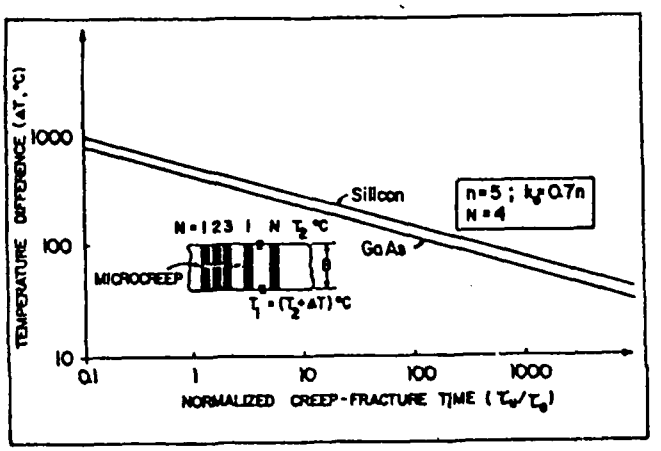


FIGURE 3: NORMALIZED CREEP FRACTURE TIME VS. DIFFERENTIAL TEMPERATURE

Consider a thin layer of the stressed materials of width B. Let T_1 and T_2 be temperatures at the two extremities of the layer as shown in Fig. 3, where $T_1 > T_2$. The test material being composite in nature, the analysis is done by dividing the layer into N strips. Due to the temperature difference, the thermoelastic stress and strain at the i^{th} strip can be represented by the quantities σ_i and ε_i, respectively. If δ_i is the

elongation of the i^{th} strip, then the basic equations of equilibrium are:

$$\sum_{i=1}^{N} \left(\frac{N+1-i}{N}\,\sigma_i\right) = \sum_{i=1}^{N} \varepsilon_i\,\alpha_i\,\Delta T \equiv Q_A \qquad (7)$$

where ΔT is the temperature difference, (T_1-T_2). E_i and α_i are the Young's modulus and coefficient of thermal expansion of the i^{th} strip respectively.

The strain-displacement relation can be specified as

$$\varepsilon_i = \delta_i / B, \qquad (8)$$

together with the compatibility condition,

$$\delta_i = \frac{N+1-i}{N}\,\delta_1 \quad . \qquad (9)$$

Further, the constitutive equations of creep initiation and growth are given by [10]:

$$\varepsilon_i = (\sigma_i/\varepsilon_i) + \varepsilon_c \qquad (10a)$$

$$d\varepsilon_c/dt = C_1\,(\sigma_i/1-q_i)^{n_o} \qquad (10b)$$

$$dq_i/dt = C_2\,(\sigma_i/1-q_i)^{k_o} \qquad (10c)$$

where C_1, C_2, n_o and k_o are material constants and ε_c is the creep-strain. The quantity q is a damage parameter which increases from zero in a virgin state to unity at rupture. For most of the materials [10], the value of n_o is less than 5 and k_o is nearly equal to 0.7 n_o.

When a continuous body occupying a volume V is acted upon the surface by a certain stress, the constitutive factor concerning steady creep behavior would be monotonic. That is, increases in stress would cause increases in the strain rate. For a steadily creeping material, the growth law of damage can be written as [10],

$$d\varepsilon_c/dt = d\Omega_{k_o}/dt \qquad (11a)$$

and

$$dq/dt = C_2\,\phi^{k_o}(\sigma) / (1-q)^{k_o} = \Omega_{k_o}(\sigma) / (1-q)^{k_o} \qquad (11b)$$

where $\Omega_{k_o}(\sigma) = C_1\,\phi^{k_o}(\sigma)$ and $\phi(\sigma)$ is a scalar invariant of the stress function, σ [10].

Further, the specific rate of work done in the creep process or the strain energy dissipation can be written as

$$\zeta(t) = \frac{1}{V}\iiint (1-q)^{k_o+1}\,dV. \qquad (12)$$

Integrating the damage relation dq/dt of equation (11) over the volume of the body (V) and combining with equation (12) the following result is obtained:

$$(-1/k_o+1)\,d\zeta(t)/dt = \frac{1}{V}\iiint \Omega_{k_o}(\sigma)\,dV \quad . \qquad (13)$$

The growth damage as decided by the above relation would culminate at a critical stress level of statically admissable value and then the rupture will take place. Initially, q = o throughout the body; that is, $\zeta(o) = o$. At final rupture, $t = \tau_U$, $\zeta = \zeta_U > 0$. Hence by integrating equation (13) over the time interval $(0, \tau_U)$, the upper bound on life time is obtained as,

$$\tau_U \leq V(1-\zeta_U) \,/\, [(1+k_o)\iiint C_1\,\phi^{k_o}(\sigma)\,dV] \quad . \qquad (14)$$

The steady-state stress for the multiple strip structure (Fig. 3) is given by [10]

$$\sigma_i = [(N+1-i)/N]^{1/n_o}\,Q_A/I_{n_o}(N),\ i = 1,2,3... \qquad (15)$$

where

$$I_n(N) = \sum_{i=1}^{N} [(N+1-i)/N]^{1+1/n_o}.$$

The corresponding upper bound of normalized rupture time can be estimated as [11]:

$$\tau_U/\tau_o = F_U(k_o) \,/\, (\sigma/\sigma_o)^{k_o} \qquad (16)$$

where τ_o is the rupture time of a single strip under the tensile stress σ_o and $\sigma = \alpha E\,\Delta T$; further,

$$F_U(k_o) = N\left\{\sum_{i=1}^{N} [(N+1-i)/N]^{k_o/k_o-1}\right\}^{k_o-1} \quad . \qquad (17)$$

The variation of normalized creep-failure time as a function of temperature difference for a typical deteriorating semiconductor structure (thin layer) is shown in Fig. 3. Silicon and GaAs are taken as the test materials, and the failure is presumed to occur when the creep reaches the fourth strip (that is, N = 4).

Work is in progress to estimate latent damage time due to creep propagation to vulnerable sites. This is done by evaluating the severity of zaps and the lethality of the effect. The lethality will be measured in terms of the creep failure time quantified by equation (16).

Further, the average number of zaps per unit time required to cause a latent failure will be determined by a systematic accelerated aging procedure based on an algorithm formulated on the principle of equivalent aging. The aging of the test device will be assessed by deviatory leakage current and/or nonlinear transfer characteristics of the device.

CONCLUSIONS

A possible mechanism of latent failure due to electrical overstressing in microelectronic devices is the time-dependent (cumulative) thermoelastic response of the device medium. That is, latent modes of failure can be attributed to the creeping of microflaws in the active locales of the device leading to deviatory performance characteristics. The thermoelastic response of

the device is governed by both the thermodynamic inhomogeneities of the medium as well as by the pulsating/transient nature of the external stimuli. The present theoretical analysis on creep percolation can supplement the (latent mode) failure analysis based on micrographic studies of failed devices; hence the statistical prediction of latent failure time is possible with the data acquired via accelerated tests and calculations based on the equivalent aging principle.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Among the LSI devices, MOS circuits are highly sensitive to damages due to electrical overstressings (EOS) arising from electrostatic discharges (ESD). Hence, several schemes have been developed for LSI input protection (on-chip) circuits. However, it has been observed that, if repeated, and/or multiple discharges occur, the protection circuits themselves would be cumulatively stressed, with the result that their protection capability will be degraded progressively. At a particular

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stage, the ineffectiveness of the protection circuit will allow subsequent stress occurrences ("zaps") to reach the active MOS regions causing a total device failure. Considering various component-damages ("woundings") observed at the protection networks, the cumulative degradation at low or subcatastrophic thresholds of static exposure can be modeled by an appropriate aging process with relevant statistics as indicated in the present work.

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NOTE

SUSCEPTIBILITY OF ON-CHIP PROTECTION CIRCUITS TO LATENT FAILURES CAUSED BY ELECTROSTATIC DISCHARGES

(Received 26 August 1985; in revised form 2 November 1985)

INTRODUCTION

Among the LSI devices, MOS circuits are highly sensitive to damages due to electrical overstressings (EOS) arising from electrostatic discharges (ESD). Hence, several schemes have been developed for LSI input protection (on-chip) circuits [1, 2]. However, it has been observed that, if repeated, and/or multiple discharges occur, the protection circuits themselves would be cumulatively stressed, with the result that their protection capability will be degraded progressively [3]. At a particular stage, the ineffectiveness of the protection circuit will allow subsequent stress occurrences ("zaps") to reach the active MOS regions causing a total device failure. Considering various component-damages ("woundings") observed at the protection networks, the cumulative degradation at low or subcatastrophic thresholds of static exposure can be modeled by an appropriate aging process with relevant statistics as indicated in the present work.

AGING MODEL

On-chip protection circuits which provide a low impedance path for surge voltages consist either singly or as a combination of the following basic structures [3]: (i) Polysilicon or N^+ (diffused) resistors; (ii) thin or thick oxide transistors; (iii) field-plate diodes; and (iv) punch-through devices. Low-level discharges at these protection elements may not cause the threshold-power dissipation required for catastrophic damages such as junction burnouts, oxide punchthrough and/or metallization burnouts [3]. However, repetitive, subcatastrophic occurrences of ESD can possibly induce stressings which may cause electrothermal-based "woundings" (or damage such as electromigration of metals [1, 3], thermoelastic strains [4], oxide pin-hole formation [1–3], etc.). Cumulative buildup of damage with the recurrence of stresses amounts to a dormant stage of failure during which the circuit would exhibit a performance degradation. Ultimately, the deviant performance would lead to catastrophic conditions.

The time-dependent degradation or aging can be assessed by measuring the time variation of a nondestructive property (p) related to the aging of the circuit. Suppose two time-variation curves are obtained corresponding to two distinct (subcatastrophic) stress-levels. The functional form of p is assumed independent of the stress magnitude and the two curves will have the same shape, but different length (along the time axis) as shown in Fig. 1. The times corresponding to some fixed value of p under two distinct stress levels are t_1 and t_2 (Fig. 1) and are known as "equivalent times" [5]. The "equivalent-aging principle" [5], assumes that

$$V_1^n t_1 = V_2^n t_2 = K_1 \text{ (Constant)} \qquad (1)$$

where n is the endurance coefficient. Equation (1) can also be written in terms of the average numbers of "zaps" (number of stress occurrences) Z_1 and Z_2 assumed proportional to the periods t_1 and t_2 as

$$V_1^n Z_1 = V_2^n Z_2 = K_2 \text{ (Constant)}. \qquad (2)$$

Thus, from eqn (1) or (2), for a given value of p, the corresponding value of failure-time (or average number of stress occurrences during the period of failure-time) can be assessed by determining the values of n and the constant K_1 or K_2.

CASE STUDY

For test studies, EPROMS fabricated with N-channel, silicon-gate technology are considered and the following test results due to Chase [6] are analyzed: The device was stressed at different severity (stress) levels ($V = \pm 1000$ V and ± 300 V) by a transient discharge

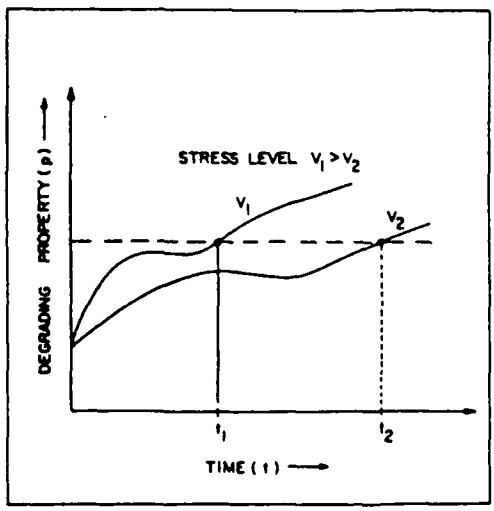


Fig. 1. Unspecified degrading device characteristics (p) vs aging time for two distinct stress levels V_1 and V_2.

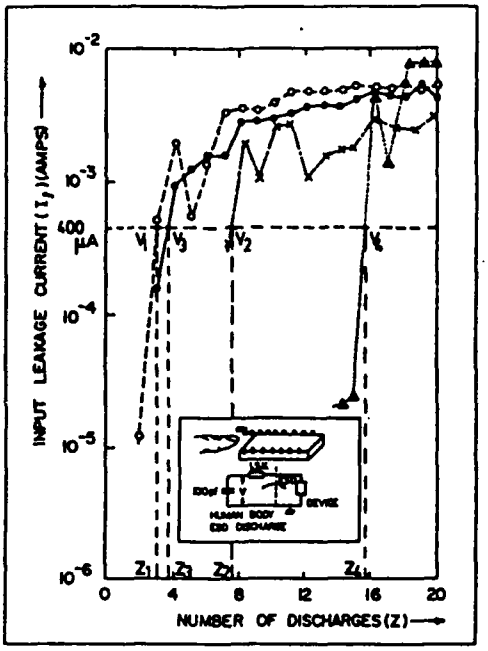


Fig. 2. Input leakage current as a function number of static discharges at a sensitive pin. Test results by simulating the zaps via equivalent human body RC-network model [6], ●—●—●, V = +1000 V; ○—○—○, V = −1000 V; ▲—▲—▲, V = +300 V and X—X—X, V = −300 V chip details are given in [6].

from an RC-network as shown in Fig. 2. (The RC-network chosen simulates the ESD from a human-body [6].) Stressing was done at a sensitive pin and the performance-degradation was monitored by measuring the input leakage current (I_l). Device failure was assumed when I_l exceeded 400 μA. The relevant results are shown in Fig. 2. The endurance coefficient calculations [eqn (2)] (based on the criteria that the critical leakage current (I_{lc}) exceeded 400 μA), yields n = 1.390 and 0.704 for positive and negative values of V, respectively. (Relevant calculation uses data points namely V_1, V_2, V_3, V_4 & Z_1, Z_2, Z_3, Z_4 shown in Fig. 2.)

LIFE-TIME STATISTICS

The device reliability relevant to the degradation-performance under repetitive stressings can be modeled by assuming that degradation rate is proportional to the existing degradation [7]. The proportionality constant is a positively distributed random variable. Then the extent of degradation would tend to be asymptotically log-normal. Hence, the general form of life distribution in terms of Z (number of stress occurrences) is given by [7].

$$G(Z, y_c) = 1 - \phi\left[\frac{\ln(y_c) - \mu}{\sigma}\right] \qquad (3)$$

where ϕ is the standard normal distribution and $y_c = (I_l - I_{l_0})$. Further, $\ln(y_c)$ has the mean value of μ and a standard deviation equal to σ. From the data pertaining to stress level of +1000 V of Fig. 2, the presumed log-normal fit [eqn (3)] is demonstrated in Fig. 3 where the quantity h_c refers to $\ln(1 - \phi)^{-1}$.

CONCLUDING REMARKS

The existing works on protection network reliability are invariably concerned with catastrophic failures [3, 8]. The lack of analyses on latent damages prompted the present investigations. The approach indicated here provides an algorithmic support based on "equivalent aging principle" to analyze the test data on latent failures. The study reveals the applicability of lognormal distribution to the statistics of aging process of the protection circuits.

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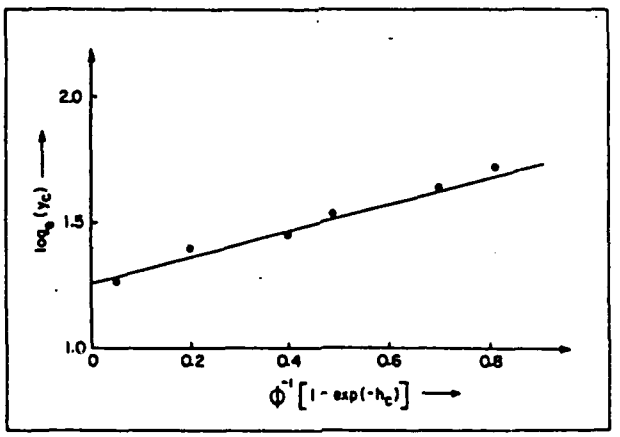


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MOS SCALING EFFECTS ON ESD-BASED FAILURES

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ABSTRACT

VLSI/ULSI strategies applied to MOS devices shrink-down the active dimensions to extremely small magnitudes and warrent unique modeling of the device-response under electrical overstresses (EOS) caused by external influences like electrostatic discharge (ESD), electromagnetic pulsing, etc. The resulting adverse effects can manifest in two failure modes, namely, the catastrophic damage and endochronic degradation. The impact of scaling-down on device failures is deduced in terms of EOS parameters and device-dimensions.

INTRODUCTION

A new type of contaminant that plagues the modern microelectronics industry is the triboelectric static accumulation and discharge through semiconductor devices.[1] Especially among all devices, the component most sensitive and susceptible to damages arising from electrostatic discharge (ESD) is the metal-oxide semiconductor; high electrostatic potential build-up often renders the MOSFETs to fail completely (catastrophic damage) or to show performance degradation as a result of deteriorations in the dielectric integrity and oxide-silicon interface under ESD environments.[2]

With the scaling-down imposed by shrinking geometrical requirements designed to obtain improved device characteristics and increased packaging density, the gate-region of the MOSFET has become even more vulnerable to ESD-based failures caused by two major geometrical factors, namely, (a) scaling the gate-oxide thickness to ultra thin dimensions (about 100Å) results in an extremely high field intensity in the dielectric approaching the limits of breakdown conditions[3,4] and (b) geometrical reduction leading to shortened channel length and narrowed channel width can augment the possibilities of electrical overstressing due to external transients.

Thus the net effect of shrunk geometry would be to enhance the susceptibility of the device to ESD-based failures with two possibilities: The first one would refer to irreversible (catastrophic) gate-oxide (dielectric) breakdown due to the impulsive ESD zap at the gate terminal.[4] The second type of damage would pertain to slow (time-dependent) performance degradation resulting from sub-catastrophic zaps; when such low-level transients occur repeatedly, endochronic build-up of interface-states, trapped charges in the bulk-dielectric, etc., would occur due to the field-induced injection and/or impact ionization phenomena in the oxides.[5] The purpose of the present investigations is to analyze the performance degradation failure of a MOSFET under various severity levels of ESD zaps and to evaluate the corresponding extent of lethality in quantifiable terms via appropriate models depicting the various modes/mechanisms of ESD interaction with the infrastructure of the device. Hence, the role of geometrical parameters in deciding the lethality/survivability of the device subjected to ESD transients (single or repetitive) is elucidated. This analysis would form the basis to assess the device reliability as a function of scaling-down strategies.

ANALYSIS

The ESD phenomena normally encountered can be simulated by three well-established models, namely,[6] (a) human-body model, (b) charged-device model, and (c) field-induced model. The human-body model (Fig. 1) depicts the transfer of static from a charged individual to ground via the test device.

Charged-device[7] model represents the bleed-off of accumulated charge upon the device-surface to ground through the pin and conductive parts of the active device (Fig. 2). The third model simulates the effect of the charge distribution and discharge when a device is exposed to a static-electric field (Fig. 3).

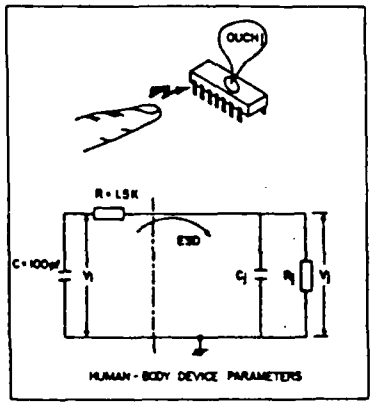


FIG 1 : HUMAN-BODY MODEL

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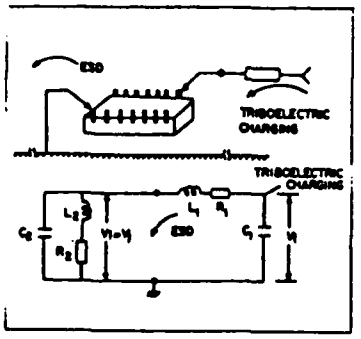


FIG 2 : CHARGED-DEVICE MODEL

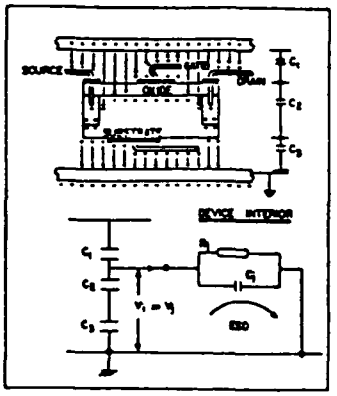


FIG 3 : FIELD-INDUCED MODEL

In the event of a high intensity ESD at the gate of a MOS device, a dielectric breakdown is likely to occur in the thin gate-oxide film. This breakdown process may be divided into two stages: During the first or build-up stage, localized high-field current density are formed as a result of charge-trap generation with accompanied barrier lowering. Eventually when the local current density or field exceeds a critical value, the rapid runaway stage begins during which additional runaway (electrical and/or thermal) process result in breakdown.

The field-controlled breakdown essentially depends on the intrinsic breakdown strength (~8MV/cm) of the oxide and is primarily dictated by the Fowler-Nordheim[3] tunneling of electrons from the conduction band of Si substrate into the oxide. The corresponding current density (J) is approximately equal to $AE^2 \exp(-B/E)$ where A and B are constants with (approximate) values of 2×10^6 amperes/$(MV)^2$ and 238 MV/cm, respectively.[8] The oxide-defects also would significantly influence the breakdown mechanism.

Tunneling of electrons from Si into the oxide is followed by transport of these charges in the oxide with the creation of electron-hole pairs by the interaction of field-accelerated electrons with the oxide via impact ionization. This may lead to local dissipation of energy from the excited carriers into heat through excitation of lattice vibration mode; if this joule heating is not extracted fast enough by conduction, the local temperature would rise until a permanent damage occurs, as observed by Yamabe, et al.[9]

The critical voltage or severity level of catastrophy at which irreversible gate-oxide damage would occur can be formulated in terms of EOS parameter(s) and the vulnerable geometries of the device as follows:

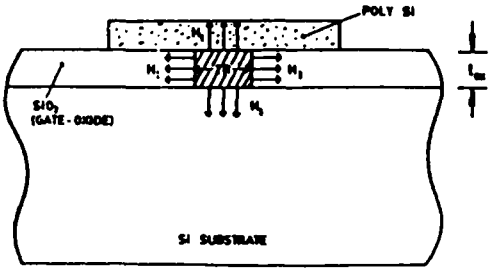


FIG 4 HEAT-FLUX ACROSS THE GATE-OXIDE

Considering a cylindrical current path from Si substrate to the polysilicon electrode across the gate-dielectric (Fig. 4), the heat-flux (H) in the current path into the Si substrate can be written as

$$H_1 = 2\pi R^2 K_{Si} \Delta T / \Delta x_{Si}, \text{ and} \quad (1)$$

$$H_2 = 2\pi R t_{ox} K_{SiO_2} \Delta T / \Delta x_{SiO_2} \quad (2)$$

where K and Δx are thermal conductivity and thermal diffusion width, respectively. Further, ΔT is the temperature rise, R is the radius of current path and t_{ox} is the gate-oxide thickness. In terms of electric power dissipated as heat, the critical voltage (V_c) of oxide breakdown can be obtained from the following relation:

$$\sigma V_c^2 / t_{ox} = H \text{ (per unit area)} \quad (3)$$

where σ refers to the electrical conductivity of the oxide-film. For steady-state temperature rise (ΔT_∞),

$$V_c = [K_{Si} \Delta T_\infty t_{ox} / (\Delta x_{Si} \sigma)]^{1/2} \quad (4)$$

For the transient condition governed by the narrow pulse regime of the ESD events, the thermal conduction equation for the dielectric gate can be written as

$$C\rho d(\Delta T)/dt - \nabla.[K_{SiO_2}(\nabla T)] + \sigma E_c^2 \quad (5)$$

where E_c is the critical breakdown field, C and ρ refer to the specific heat and mass density of the oxide material, respectively. For a pulse duration of W, the critical voltage of breakdown V_{cw} can be obtained from the principal solution of Eq. (5). It is given by

$$V_{cw}(x,t) = [K_{Si} t_{ox} \Delta T_w / (\sigma \Delta x_{Si})]^{1/2} \quad (6)$$

where $\Delta T_v = \Delta T_m[1-\alpha(x,t)]$. Here $\Delta T_m(x)$ is equal to $\sigma E_c^2 [t_{ox}^2/4-x^2]/2K_{SiO_2}$ and

$\alpha(x,t)=1-\sum_{n=1}^{\infty}(-1)^n\{\int_0^{\nu}(\text{erf } x^- + \text{erf } x^+)dt\}$ where x is the hot-spot under observation. Further $x^- = [2n+1)t_{ox}/2 \mp x]/2\sqrt{a_{SiO_2}t}$ where a_{SiO_2} is the thermal diffusivity of the oxide.

Thus Eq. (6) evaluates the critical voltage in terms of the ESD parameters (E_c and W) and the device geometrical (scaling) quantity, namely, t_{ox}.

It applies to the zap received by the gate from a human-body (Fig. 1) or a charged-body (Fig. 2). It is analogous to the popular Wunsch-Bell relation[10] specified for junction devices to calculate the critical power dissipation at the junction.

Field Induced Model (Fig. 3)

A MOS device subjected to field-induced mode of electrical overstressing can be analyzed considering a dielectric plus air-gap model depicted in Fig. 5.

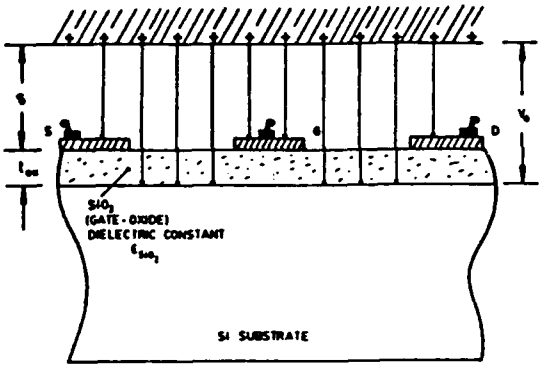


FIG. 5 FIELD-INDUCED BREAKDOWN ACROSS THE GATE-OXIDE PLUS AIR-GAP

The critical air-gap voltage V_o at which breakdown occurs and pumps the charges into the dielectric can be specified in terms of an over-voltage parameter ΔV is given by

$$\Delta V \sim C_1 t_{ox}^2 E_I/\delta(1+t_{ox}/\delta\varepsilon_{SiO_2})^2 \qquad (7)$$

where C_1 is a constant and E_I is the intrinsic breakdown strength of the oxide.

Thus the electrical overstressing pertaining to the field-induced condition may initiate a breakdown by the critical overvoltage (due to stressing) which is directly proportional to the square of the dielectric thickness and is inversely proportional to the gap width.

ENDOCHRONIC DEGRADATION

At subcatastrophic levels of stressing, the device would exhibit a latent mode of failure manifesting as the endochronic performance degradation. Such "wounded" or "rogue" components may still be functional (however, with deviatory characteristics) and are potentially prone to catastrophic failures on subsequent stress repetitions.

The aging of a device can be specified in terms of four possible damaging influences, namely, the elevated temperature, the intensive electric field, depletory electromigration and undue thermoelastic stresses. Specifically, in a MOS device, the degradation is observed in the form of shifts in the threshold voltage and/or changes in trans-conductance. When a device takes multiple (low-level) zaps at random (or regular) intervals, the net time-dependent degradation due to M stresses (zaps) can be written as follows:[11]

$$\frac{\Delta V_T}{V_T} = \{[1 + \frac{M}{1-p}(\frac{\Delta V_{T1}}{V_T})^{1/2}]^{1-p} - 1\}^r$$

and

$$\frac{\Delta g_m}{g_m} = \{1 + \frac{M}{1-p}\frac{\Delta g_{m1}}{g_m}^{1/2}]^{1-p} - 1\}^r \qquad (8)$$

where V_T and g_m refer to the threshold voltage and the transconductance, respectively. Further, p is a constant (<1) and the exponent r is greater than one. ΔV_{T1} and Δg_{m1} are the changes in V_T and g_m (respectively) for a single zap. In general, ΔV_T or Δg_m is determined by the magnitude and sign of the charge injected into the dielectric. Typical variation (measured) of $\Delta g_m/g_m$ as a function of number of zaps is presented in Fig. 6.

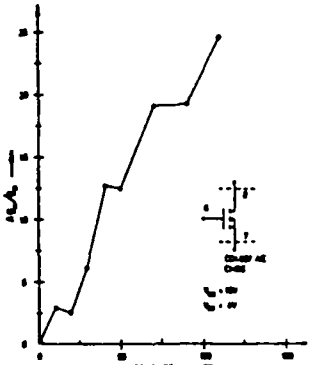


FIG 6 TRANSCONDUCTANCE DEVIATION AS A FUNCTION OF NO OF ZAPS

Changes in g_m or V_T is mainly controlled by the trapped carrier density N(t) given by[12]

$$N(t) = N_T\{1-\exp[-\sigma N_{inj}(t)]\} \qquad (9)$$

with $N_{inj}(t) = (1/q)\int_0^t J_{inj}(t')dt'$. Here σ is the charge accumulation coefficient and J_{inj} refers to the injected current density.

The effect of scaling down on the performance degradation will be implicitly determined by the injected current density. That is, for given operating potentials, the scaling down would alter the field intensity (magnitude and pattern) at the active regions with the corresponding changes in the magnitude of injected current density. Hence the degradation of the device would be influenced by the alterations in all the major three device (geometrical) parameters, namely, the channel length, the channel width, and the oxide thickness, inasmuch as all these parameters individually or collectively decide the field that controls the current injection phenomenon.

CONCLUSIONS

From the analyses indicated here, the following conclusions can be inferred:

1. For an ESD addressed to human-body model and/or charge-device model, the critical breakdown voltage of the oxide is approximately proportional to $\sqrt{t_{ox}}$.

2. The corresponding damage is also controlled by the overstressing parameters, namely, the stress level and the pulse-width of the transient.

3. When the overstressing refers to field-induced model of Fig. 3, the excess voltage required for the breakdown to take place and hence for the injection of charges into the dieletric, is proportional to t_{ox}^2 and decreases with the increasing gap-width.

4. The time-dependent degradation due to subcatastrophic and repetitive stresses can be specified by the endochronic changes in g_m or V_T (Fig. 6). The growth of degradation would depend essentially on the initial value of damage caused by a single zap and the time-dependent increase would be decided by the number and rate of subsequent zaps. (Eq. 8).

5. The performance deviation caused by a single zap would be determined by the cohesive influence of current pumping due to the field within the device infrastructure; and this field is a function of the geometrical parameters, namely, the channel width, the channel length, and the gate-oxide thickness. Any scaling-down strategy would thus directly alter the single-zap damage ($\Delta g_{m1}/g_m$ or $\Delta V_{T1}/V_T$) which initiates the endochronic derivatory response.

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SUSCEPTIBILITY OF PCB-MOUNTED MICROELECTRONIC DEVICES TO FAILURES CAUSED BY ELECTROSTATIC DISCHARGES

Susceptibility of PCB-mounted devices to failures caused by electrostatic discharges (ESD) is studied. Theoretical analysis and a simulated experiment indicate higher vulnerability of subassembled (PCB-mounted) devices relative to their unmounted (isolated) counterparts.

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Transference of electric charges from one moving surface to another by forces created by the heat of friction induce static electricity causing a potential difference between the surfaces involved. The static voltage on nonconductors commonly reaches magnitudes of 500 V to 1500 V under

relatively high humidity conditions and often as high as 15,000 V TO 20,000 V under dry conditions. The charges induced on a nonconductor can remain in "puddles" on the surface for hours for even days. When such a static build-up occurs in a semiconductor, the device may fail either due to excessive voltage difference or, due to the discharge of this voltage across the device causing an excessive current to flow. In either case, a damage (catastrophic or performance degradation) in the device is likely to occur in the sensitive parts of the devices.

Thus electrostatic discharge (ESD) plagues the modern microelectronic industry as a new contaminant and poses unique reliability problems due to "sneaky" failures in production lines, in the inspection departments, at the stock-room, while-on-transit or in the hands of the customers.

In general, such ESD threats are conceived as and supposedly experienced only in isolated devices; that is, in those devices which are not subassembled or mounted on a PCB. This presumption is rather incorrect and as pointed out by Donald Frank (Ref. 1), it is a "myth" to presume "an ESD sensitive component cannot be damaged once it is installed on a circuit board." Notwithstanding, in the existing practice, survivability assessment of electronic systems under electrical overstresses (EOS) arising from electrostatic discharges (ESD) have been invariably restricted to analyzing the isolated components only; and, failure prevention measures (Ref. 2) have been prescribed acordingly in respect of handling and using isolation devices. Further, failures threshold studies and protective circuit designs have also been based mostly on the anticipated ESD threats exclusive to unmounted/isolated devices only.

However, case studies (Refs. 1, 3 & 4) reveal that devices mounted on printed circuit boards (PCB) would experience high failure rates under ESD environments despite exercising the prescribed precautionary measures. For example, as indicated by William Thompson, (Ref. 3) non-observance of ESD protective measures in handling and using certain costly replacement subassemblies of tactical systems like missiles, resulted in excessive loss and warranted frequent field-repairs.

Not taking care to protect ESD sensitive components from the damage after they have been installed in an equipment can also result in performance degradation of the unit, as pointed out by Donald Frank (Ref. 1) referring to a case of a scientific calculator being not able to retain the programmed memory when necessary handling procedures were not followed.

More evidence on ESD-induced damage to integrated circuits on PCB's has been recently furnished by Shaw and Enoch (Ref. 4) with experimental data pertaining to the sensitivity of a batch of octal-latch integrated circuits mounted on a printed circuit board to ESD transients. Their experiments reveal the high static propensity of PCB's would lead to an ESD transient, sufficiently large enough to cause catastrophic damages in mounted devices.

In order to assess, the proneness of PCB-mounted devices to failures under ESD-based overstresses, it is essential to formulate a systematic model so as to estimate the relative lethality of such devices (in the subassembly) in comparison with that of isolated (unmounted) counter parts. A typical model can be conceived as follows:

THEORETICAL MODEL

Referring to Fig. 1, the electrostatic discharge from a human body onto a PCB-pin is equivalently represented by a network. The components of the dual-RLC network (Ref. 5 & 6) (namely R_B L_B C_B & R_H L_H C_H) denote the body and the hand, and the voltage V_i on C_B depicts the electrostatic voltage on the body. The transmission-line path between the PCB-pin and the device-pin is represented by an equivalent T-network (Ref. 6) with lumped elements of L_e and C_e. The device junction under stress is assumed to be purely resistive (R_j) and is shunted by substrate/packaging capacitance, C_j. Associated with R_j is the effective junction area (A) through which the bulk of the ESD current is passed. Typical values OF R_j, C_j, and dual-RLC elements are shown in Fig. 1. Further, the path-length of the PCB transmission-line is assumed as 5 cm (a typical value) with a characteristic impedance of 50Ω. The corresponding L_e and C_e values (Ref. 7) per unit length are 2.5 nH/cm and 1 pF/cm, respectively, if the PCB has a dielectric constant of 2.5.

Analysis: The transient voltage $V_j(t)$ across the device junction is computed by Laplace transform technique, assuming a stress voltage of V_i = 1000 V. The device considered is of silicon material with A = 1000 sq. microns. For a known (computed) $V_j(t)$, the average power per unit junction area, namely, P(PCBM-D) as a function of time is plotted in Fig. 2. To find a measure for the damage (as implied by junction melting), the junction

power per unit area at the melting point of the device medium (silicon), denoted as P(W-B), is computed as a function of time via well-known Wunsch-Bell (Ref. 8) heat transfer equation. The relevant results are also presented in Fig. 2.

The condition for catastrophic failure of the PCB-mounted device is that $P(PCBM-D) \geq P(W-B)$. From Fig. 2, this failure condition corresponds to the time, $t = \tau_1 = 4$ nsec. If the test device considered were to be an isolated piece (instead of being mounted on a PCB), the corresponding junction power per unit area, P(I-D) as a function of time, can be calculated (Ref. 5) by the equivalent network of Fig. 1 with the omission of transmission line and inductive parameters. The results are shown on Fig. 2 with the associated failure time being $\tau_2 = 9$ nsec. Hence the relative lethality endurance (Ref. 9) of the PCB-mounted device in comparison with an isolated device is given by (Ref. 9) $\tau_1/\tau_2 = 0.44$. That is, for a given severity level of ESD, the PCB-mounted device has an endurance capability (Ref. 9) of only 44% of that of an isolated device. The enhanced lethality and higher proneness to failure of the PCB-mounted device results from current-peaking effects (Ref. 10) due to inductive elements of the equivalent circuit shown in Fig. 1. The super-fast initial-voltage spike across R_j is indicated by the overshoot curve of V_j (PCBM-D) would pose a higher severity, as experienced in the reported case studies (Ref. 1, 3, & 4).

EXPERIMENTAL STUDIES

To understand the implications of current-peaking effects due to the inductive elements of the transmission-line on the PCB, an experiment simulating the equivalent circuit of Fig. 1 was constructed using a PCB with 5cm long parallel line, terminated by a parallel combination of R_j = 100 ohm and C_j = 5pF. The typical output-discharge voltage waveforms, with and without the transmission-line, as observed on a wide-band oscilloscope are shown in Figs. 3 A & B. These waveforms closely depict the computer-simulated discharge profiles of Fig. 2. The characteristic initial peak (due to the inductive elements of the transmission line) of Fig. 3A can drive the junction into the Wunch-Bell's limit of catastrophy (Ref. 8). But when the inductive elements are absent (that is, when the device is considered as an isolated component), the discharge waveform is essentially an RC transient curve without initial peak(s)/overshoot(s) as could be observed from Fig. 3B. Thus the simulated experiment supplements the concept that the ESD threat could be higher when the components are on a PCB than when the components experience the ESD zap as isolated devices.

Remedial Measures: In spite of exercising ESD controls (Ref. 2) during design, test, manufacture, assembly and packaging for delivery, etc., there persists an enhanced threat of failure in respect of replacement assemblies (PCB) as indicated in the present analysis. Therefore additional protection methods may be required exclusivly at subassembly levels. Transient suppression at subassembly level can be done by three schemes: In the first

method (Ref. 4) as recommended by some manufacturers, resistors (up to 400 ohms) can be included in series with inputs that are directly wired to off-board connectors, so as to limit discharge current of an ESD transient. Such in-line resistors have been observed to be effective in protecting ICs on a board only to a moderate extent; and also their effectiveness is dependent on the polarity of the transient, the greater effect being achieved for negative transients (Ref. 4).

Another scheme suggested here is to use a negative resistance elements (varistors) as shunt-type transient suppressors across the inputs and off-board connectors (Ref. 11). Because of the symmetrical sharp breakdown characteristics, a varistor can provide adequate bipolar transient suppression. Further, availability of surface-mounted varistors (Ref. 11) indicate their promising applications in PCB technology.

The third method (Ref. 12) of transient suppression can be achieved by using positive temperature coefficient (PTC) resistors as series elements at the input terminals. Low resistance conductive polymer-based PTC devices have been studied as overcurrent protectors (Ref. 12) and their use as protective devices for PCB-mounted components awaits the trial of experimentation.

It is suggested here that a miniature protective components compatible for PCB applications can be developed by judicious combination of in-line resistors, varistors and PTC resistors. If such a scheme is effectively implemented, the hazard-proneness of PCB-mounted devices to ESD-based overstresses could possibly be overcome.

Acknowledgement: The present study is supported by a grant by the Office of Naval Research (No. 613-005) which is gratefully acknowledged.

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CAPTIONS FOR THE DIAGRAMS:

Fig. 1: Human-body model of electrostatic discharge (ESD) through PCB-mounted devices: Equivalent circuit representation.

Fig. 2: Variations of ESD-induced junction voltage (V_j) and average power/unit junction area (P) as functions of time; V_j(PCBM-D) & P(PCBM-D) correspond to PCB-mounted device. V_j(I-D) & P(I-D) correspond to isolated device. P(W-B): Calculated by Wunsch-Bell model.

Fig. 3: Typical outputs from an ESD Simulator Depicting the Human Body Model shown in Fig. 1.

A. Reactive Elements of the PCB Transmission Line are included.

B. PCB Transmission Line is ommitted.

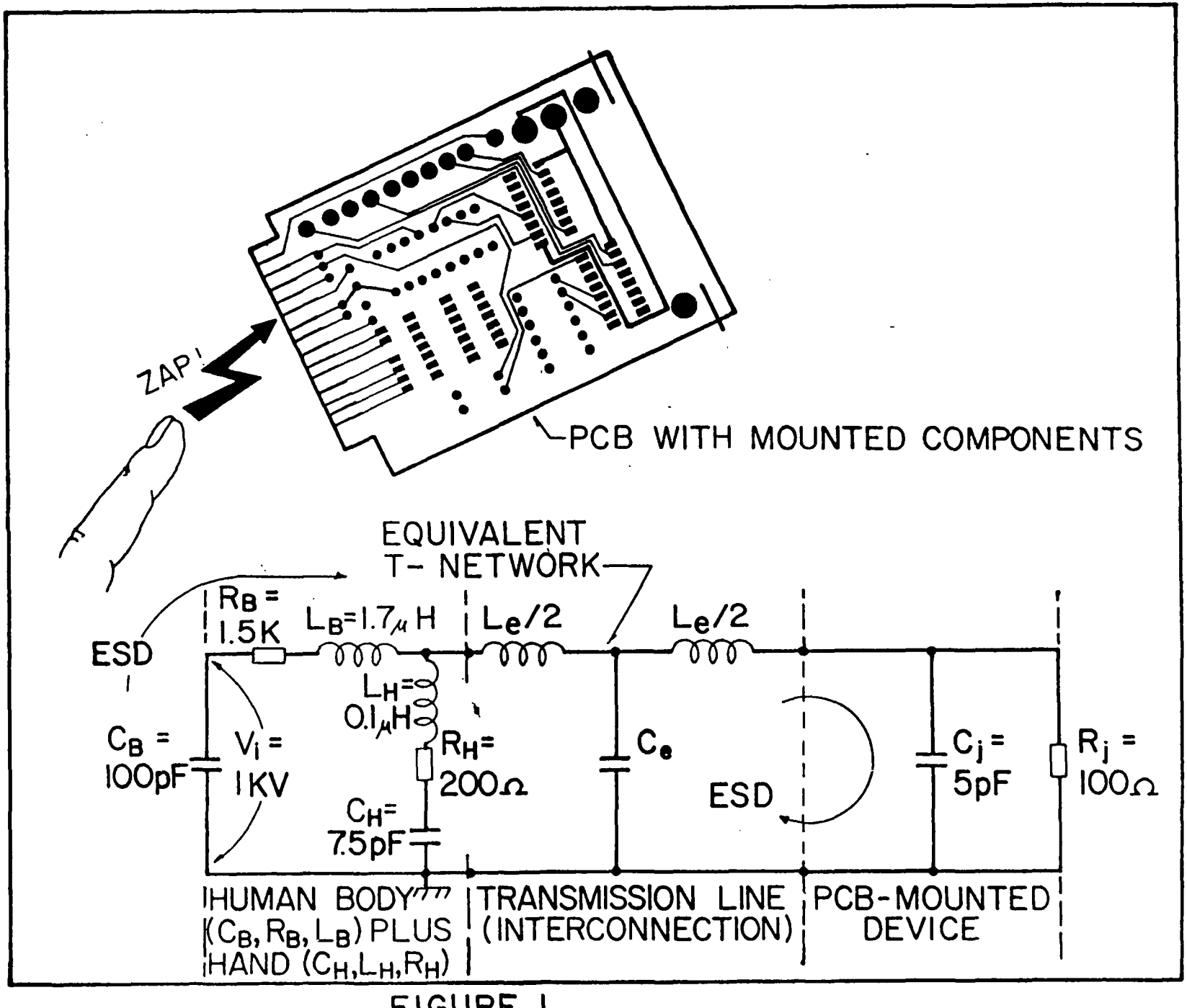

ZAP!
PCB WITH MOUNTED COMPONENTS
EQUIVALENT
T- NETWORK
ESD
R_B = 1.5K
L_B=1.7μH
$L_e/2$
$L_e/2$
L_H= 0.1μH
C_B = 100pF
V_i = 1KV
R_H= 200Ω
C_H= 7.5pF
C_e
ESD
C_j= 5pF
R_j = 100Ω
HUMAN BODY (C_B, R_B, L_B) PLUS HAND (C_H, L_H, R_H)
TRANSMISSION LINE (INTERCONNECTION)
PCB-MOUNTED DEVICE

FIGURE 1

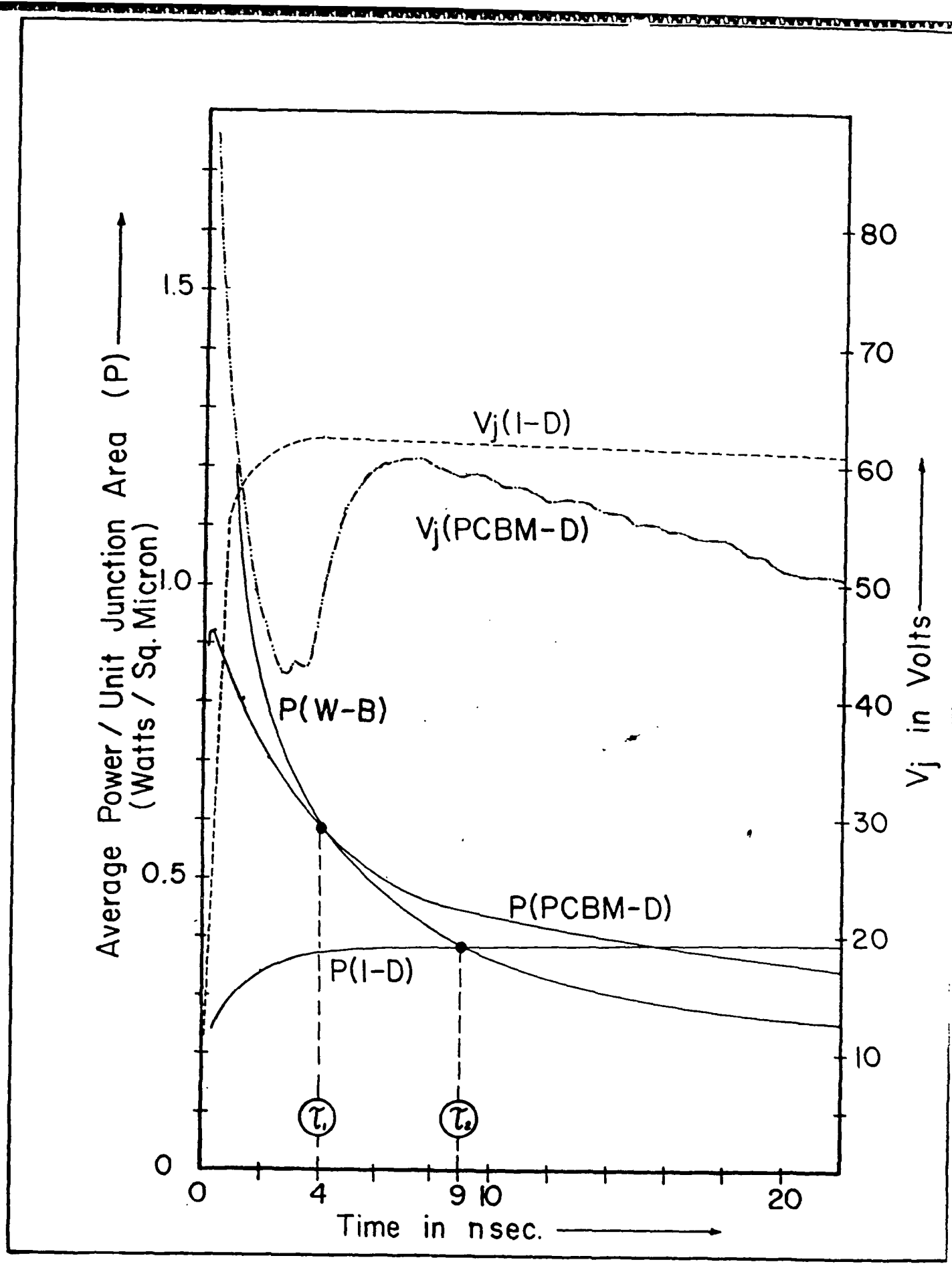
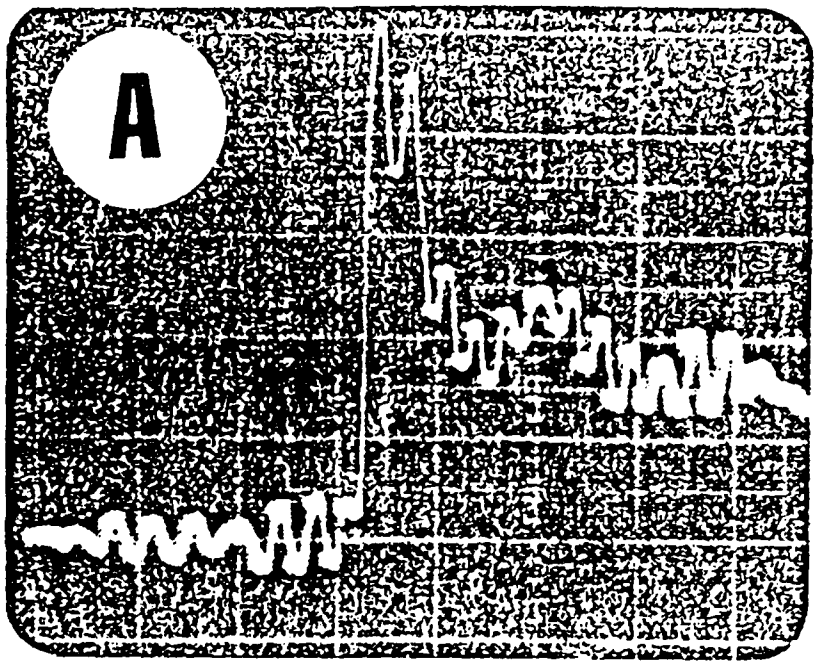
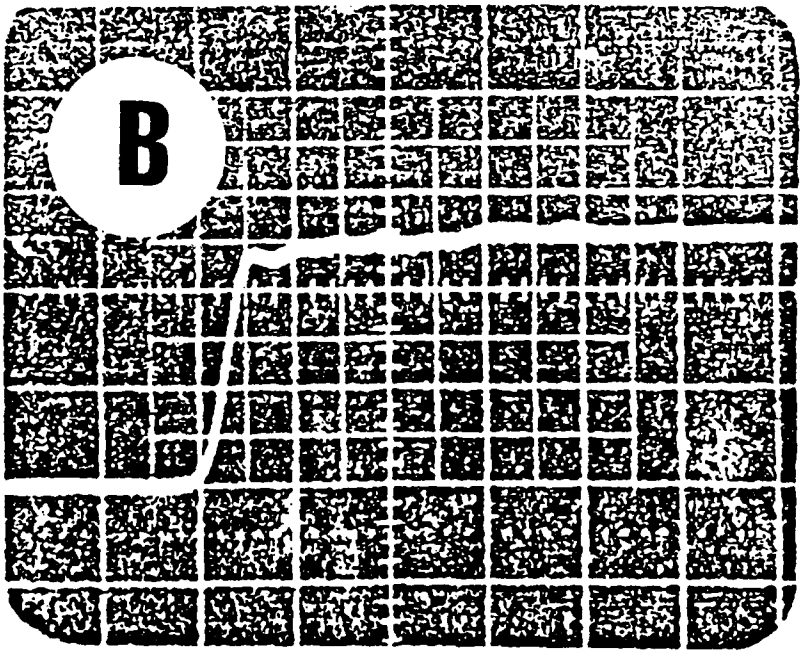

Average Power / Unit Junction Area (P)
(Watts / Sq. Micron)
1.5
1.0
0.5
0
Vj(I-D)
Vj(PCBM-D)
P(W-B)
P(PCBM-D)
P(I-D)
τ_1
τ_2
0
4
9
10
20
Time in nsec.
80
70
60
50
40
30
20
10
Vj in Volts

FIGURE 2

A



B



ESD Failures of Board-Mounted Devices

Analysis and simulated experiment indicate that mounted devices are more vulnerable to ESD than are unmounted devices.

By Perambur S. Neelakantaswamy, RIT Research Corp., Rochester, N.Y., and Rennen I. Turkman, Rochester Institute of Technology, Rochester, N.Y.

Electrostatic discharge (ESD) plagues the modern microelectronics industry and poses unique reliability problems due to failures on the production line, in the inspection department, at the stockroom, while in transit or in the hands of customers.

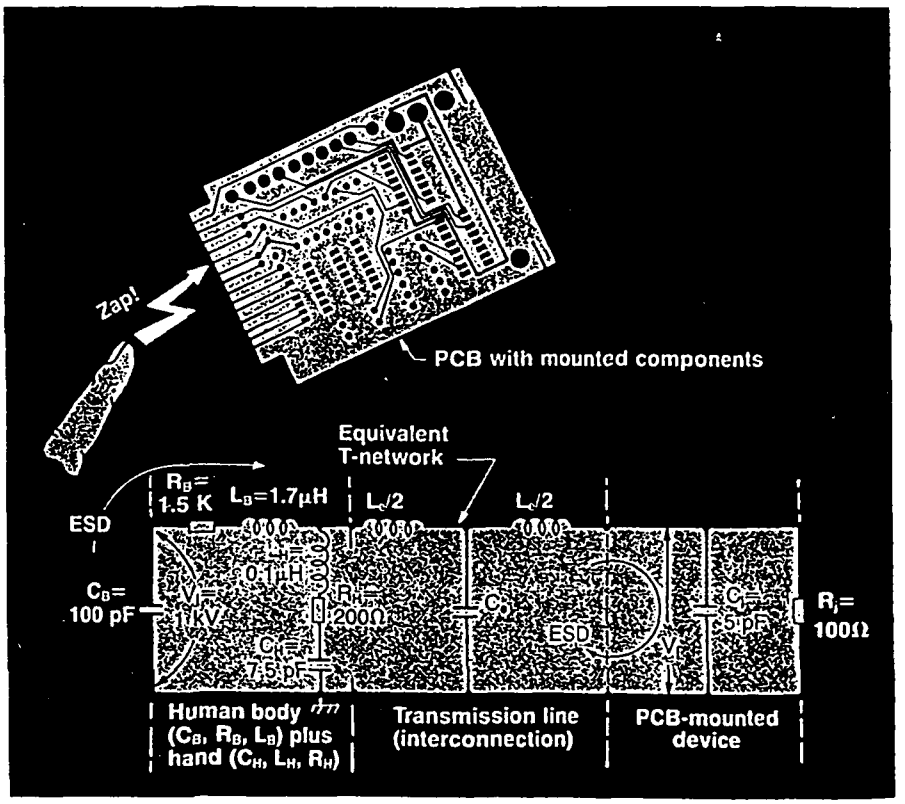
Such ESD threats are supposedly experienced only in isolated devices; that is, in devices which are not mounted on a printed circuit board (PCB). This presumption is incorrect.[1] It is a myth that an ESD-sensitive component cannot be damaged once installed on a circuit board.

Nevertheless, survivability assessments of electronic systems under electrical overstresses (EOS) arising from ESD have been restricted to analyzing isolated components only, and failure prevention measures with respect to handling and using isolated devices have been prescribed accordingly.[2] Further, failure threshold studies and protective circuit designs have also been based mostly on anticipated ESD threats exclusive to unmounted devices.

Case studies reveal that devices mounted on PCBs experience high failure rates in static-charged environments even when the prescribed precautions are taken.[1,3,4] Non-observance of ESD-protective measures in handling and using certain costly replacement subassemblies of tactical systems, like missiles, resulted in excessive loss and frequent field repairs.[3]

Not taking care to protect ESD sensitive components from damage after they have been installed in equipment can also result in performance degradation of the unit, as pointed out by Donald Frank,[1] referring to a case of a calculator that was not able to retain its programmed memory when the necessary handling procedures were not followed.

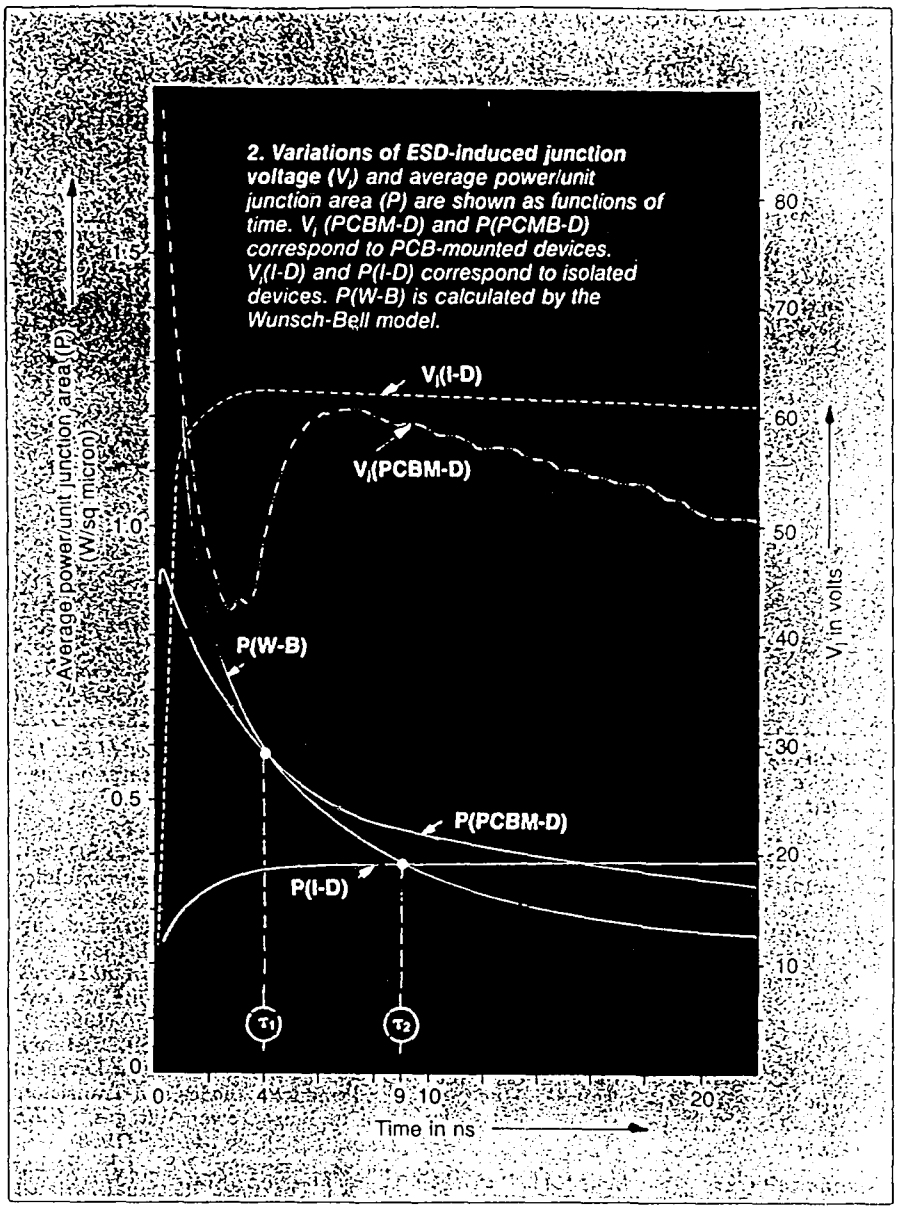
More evidence on ESD-induced damage to integrated circuits on PCBs has been recently furnished by Shaw and Enoch,[4] with experimental data pertaining to the sensitivity of a batch of octal-latch integrated circuits mounted on a printed circuit board, to ESD transients. Their experiments reveal that the high static propensity of PCBs would lead to an ESD transient, sufficiently large enough to cause catastrophic damages in mounted devices.



1. Equivalent circuit representation for a human-body model of electrostatic discharge (ESD) through PCB-mounted devices.

Theoretical model

In order to assess the likelihood of PCB-mounted devices to fail under ESD-based overstresses, it is essential to formulate a systematic model so as to estimate the relative lethality of such devices (in the subassembly) in



comparison with that of unmounted counterparts. A typical model follows.

Referring to Fig. 1, the electrostatic discharge from a human body onto a PCB pin is equivalently represented by a network. The components of the dual-*RLC* network[5,6] (namely R_B L_B C_B and R_H L_H C_H) denote the body and the hand, and the voltage V_i on C_B depicts the electrostatic voltage on the body. The transmission-line path between the PCB pin and the device pin is represented by an equivalent *T*-network[5] with lumped elements of L_e and C_e. The device junction under stress is assumed to be purely resistive (R_j) and is shunted by substrate/packaging capacitance, C_j. Associated with R_j is the effective junction area (A) through which the bulk of the ESD current is passed. Typical values of R_j, C_j, and dual-*RLC* elements are shown in Fig. 1. Further, the path length of the PCB transmission line is assumed to be 5 cm (a typical value) with a characteristic impedance of 50Ω. The corresponding L_e and C_e values[7] per unit length are 2.5 nH/cm and 1 pF/cm, respectively, if the PCB has a dielectric constant of 2.5.

The transient voltage $V_j(t)$ across the device junction is computed by Laplace transform technique, assuming a stress voltage of V_i = 1,000 V. The device considered is of silicon material with A = 1,000 sq microns. For a known (computed) $V_j(t)$, the average power per unit junction area, namely, *P(PCBM-D)* as a function of time is plotted in Fig. 2. To find a measure for the damage (as implied by junction melting), the junction power per unit area at the melting point of the device medium (silicon), denoted as *P(W-B)*, is computed as a function of time via the well-known Wunsch-Bell[8] heat-transfer equation. The relevant results are also presented in Fig. 2.

The condition for catastrophic failure of the PCB-mounted device is that *P(PCBM-D)* = *P(W-B)*. From Fig. 2, this failure condition corresponds to the time, $t = \tau_1 = 4$ ns. If the test device considered were to be an isolated piece (instead of being mounted on a PCB), the corresponding junction power per unit area, *P(I-D)* as a function of time, can be calculated[5] by the equivalent network of Fig. 1 with the omission of transmission line and inductive parameters. The results are shown on Fig. 2 with the associated failure time being τ_2 = 9 ns. Hence the relative lethality endurance[9] of the PCB-mounted device in comparison with an isolated device is given by τ_1/τ_2 = 0.44. That is, for a given severity level of ESD, the PCB-mounted device has an endurance capability of only 44 percent of that of an isolated device. The enhanced lethality and higher proneness to failure of the PCB-mounted device results from current-peaking effects[10] due to inductive elements of the equivalent circuit shown in Fig. 1. The super-fast initial-voltage spike across R_j indicated by the overshoot curve of V_j *(PCBM-D)*, would pose a higher severity as experienced in the reported case studies.[1,3,4]

Experimental studies

To understand the implications of current-peaking effects due to the inductive elements of the transmission line on the PCB, an experiment simulating the equivalent circuit of Fig. 1 was constructed using a PCB with 5-cm long parallel line, terminated by a parallel combination of R_j = 100 Ω and C_j = 5 pF. The typical output-discharge voltage waveforms, with and without the transmission line as observed on a wide-band oscilloscope, are shown in Figs. 3a and 3b. These waveforms closely depict the computer-simulated discharge profiles of Fig. 2. The characteristic initial peak (due to the inductive elements of the transmission line) of Fig. 3a can drive the junction into the Wunch-Bell's limit of catastrophe.[8] But when the inductive elements are absent (that is, when the device is considered as an isolated component), the discharge waveform is essentially an RC transient curve without initial peak(s)/overshoot(s) as could be observed from Fig. 3b. Thus the simulated experiment supplements the concept that the ESD threat could be higher when the components are on a PCB than when the components experience the ESD zap as isolated devices.

In spite of exercising ESD controls[2] during design, test, manufacture, assembly and packaging for delivery, etc., there persists a greater threat of failure of replacement assemblies (PCB) as indicated in the present analysis. Therefore additional protection may be required exclusively at subassembly levels. Transient suppression at subassembly levels can be accomplished by any one of three methods. In

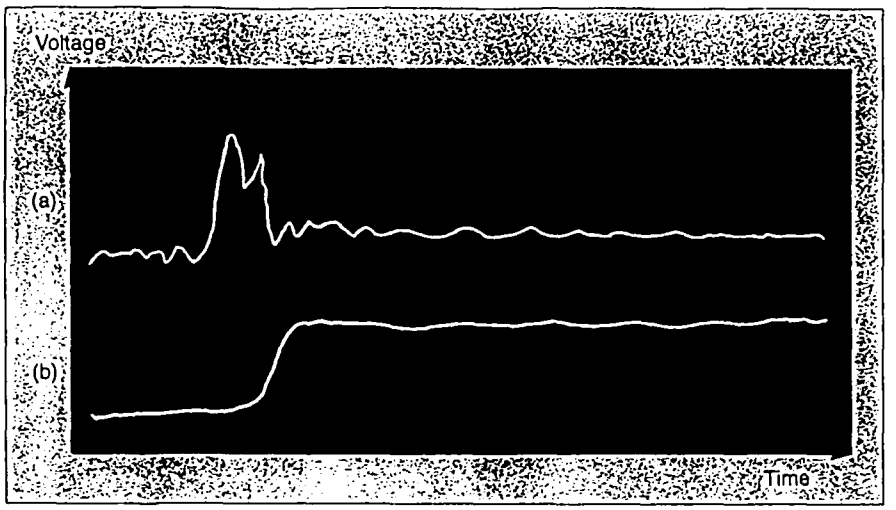
Additional protection may be required exclusively at subassembly levels.

the first method,[4] as recommended by some manufacturers, resistors (up to 400Ω) can be included in series with inputs that are directly wired to off-board connectors, so as to limit discharge current of an ESD transient. Such in-line resistors have been observed to be effective in protecting ICs on a board only to a moderate extent, and their effectiveness is dependent on the polarity of the transient.

Another scheme suggested is to use negative resistance elements (varistors) as shunt-type transient suppressors across the inputs and off-board connectors.[11] Because of the symmetrical sharp breakdown characteristics, a varistor can provide adequate bipolar transient suppression. Further, the availability of surface-mount varistors indicates their promising applications in PCB technology.

The third method[12] of transient suppression can be achieved by using positive temperature coefficient (PTC) resistors as series elements at the input terminals. Low resistance conductive polymer-based PTC devices have been studied as overcurrent protectors and their use as protective devices for PCB-mounted components awaits the trial of experimentation.

It is suggested that miniature protective components compatible for PCB applications can be developed by a judicious combination of in-line resistors, varistors and PTC resistors. If such a scheme is effectively implemented, the susceptibility of PCB-mounted devices to ESD-based overstresses could possibly be overcome. ■



3. Typical outputs from an ESD simulator depict the human-body model shown in Fig. 1: (a) reactive elements of the PCB transmission line are included; (b) PCB transmission line is omitted.

Acknowledgment

The present study is supported by a grant from the Office of Naval Research (No. 613-005).

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Electrostatic discharge

Transference of electric charges from one moving surface to another by forces created by the heat of friction induce static electricity, causing a potential difference between the surfaces involved. The static voltage on non-conductors commonly reaches magnitudes of 500 V to 1,500 V under relatively high humidity conditions and often as high as 15,000 V to 20,000 V under dry conditions. The charges induced on a non-conductor can remain in "puddles" on the surface for hours or even days. When such a static build-up occurs in a semiconductor, the device may fail either due to excessive voltage difference or due to the discharge of this voltage across the device, using an excessive current to flow. In either case, damage (catastrophic or performance degradation) is likely to occur in the sensitive parts of the devices.

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18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Electrostatic Discharge (ESD), Impulsive Electromagnetic Interference (EMI)

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Failure of equipment-mounted devices due to indirect (noninvasive) energy transfer from the ESD via transient electromagnetic coupling/interference warrants a unique modeling as detailed in this report.

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ITEM 87
INTERFERENCE TECHNOLOGY ENGINEERS' MASTER

IMPULSIVE EMI RADIATED BY ELECTROSTATIC DISCHARGES (ESD)

Failure of equipment-mounted devices due to indirect (noninvasive) energy transfer from the ESD via transient electromagnetic coupling/interference warrants a unique modeling as detailed in this article.

PERAMBUR S. NEELAKANTASWAMY, RIT RESEARCH CORPORATION, ROCHESTER, NEW YORK

Conventional studies on ESD-based damages are invariably restricted to chip-level.[1] However, there has been an increased awareness recently to investigate the susceptibility of equipment and subassemblies to ESD failures,[2,3] because such larger systems would present prominent cross-sections of exposure to impulsive electromagnetic interference (EMI) emanating from an external ESD event.[4] That is, equipment, in general, is potentially propensive to accept electromagnetic waves radiated from an external ESD occurring in the vicinity. Therefore, any sensitive device mounted within the equipment is likely to be damaged by absorbing the interfering electromagnetic energy penetrated through apertures (on the equipment-shielding) and/or coupled via conductor surfaces, connectors, etc. Eventually circuit malfunctioning and/or equipment-breakdown would occur depending on the failure being latent-type or catastrophic. Appearance of

"ghost-bits" and "bit dropouts" in computers and "sneaky" equipment failures in production lines, in the inspection departments, at the stockroom, while-on-transit or in fields, etc., can be largely attributed to such ESD-based electromagnetic influences.[5] To evaluate the cause-effect relations quantitatively in the aforesaid failure-mode, it is essential to develop an EMI model representing the ESD-excited electromagnetic wave, its coupling to devices via equipment/subassembly cross-section(s) and the resulting damage. This article proposes a model to portray exclusively the implicit (EMI-based) ESD-to-device interaction in contrast with the existing models (human-body model,[6] charged-device model[7] and field-induced model[8]) which rather describe the direct (contact-based) interactive damages.

ESD MODELS

The electrostatic discharge (ESD) phenomenon that plagues the modern electronic industry as a new contaminant, is normally simulated by three well-established models[6,7,8] describing the device to ESD interactions: The human-body model[6] shown in Figure 1 depicts the transfer of static from a charged person to ground via the test device. Charged-device model[7] (Figure 2) represents the bleed-off of accumulated charges (which "normally stay put as puddles" upon the device-surface) to ground through the pin(s) and/or conductive parts of the active device. The third model[8] simulates the effect of the charge distribution and discharge when a device is exposed to a static-electric field (Figure 3).

In general, ESD threats modeled as per Figures 1-3 are conceived and supposedly experienced only in isolated devices; that is, in those devices which are not subassembled or mounted on PCBs of the equipment. This presumption is rather incorrect and as pointed out by Frank[9], it is a "myth" to presume "an ESD sensitive component cannot be damaged once it is installed on a circuit board." Notwithstanding, in the existing practice, the survivability assessment of electronic systems under electrical overstress (EOS) arising from ESD have been invariably restricted to analyze isolated components only and failure prevention measures have been prescribed accordingly--only to the handling and using of isolated devices. Further failure threshold studies and protective circuit designs have been mostly based on anticipated ESD threats exclusive to unmounted/isolated devices.

However, case studies reveal that devices mounted on printed circuit boards (PCB) in equipment would experience high failure rates under ESD environments despite exercising the prescribed precautionary measures. For example, as indicated by Thompson,[2] non-observance of ESD protective measures in handling and using certain costly replacement subassemblies of tactical systems like missiles, resulted in excessive loss and warranted frequent field-repairs.

Not taking care to protect ESD sensitive components from the damage after they have been installed in an equipment can also result in performance degradation of the unit, as pointed out by Frank[9] referring to a

case of scientific calculator being not able to retain the programmed memory when necessary handling procedures were not followed.

More evidence on ESD-induced damage to integrated circuits on PCBs has been recently furnished by Shaw and Enoch[10] with experimental data pertaining to the sensitivity of a batch of octal-latch integrated circuits mounted on a printed circuit board to ESD transients. Their experiments reveal that high static propensity of PCBs would lead to an ESD transient sufficiently large enough to cause catastrophic damages in mounted devices.

Recently, the author has also studied[3] the susceptibility of PCB-mounted devices to failures caused by ESD and indicated the higher vulnerability of subassembled structures.

EMI MODEL

In ESD problems related to subassembled and/or equipment-mounted devices, the threat would arise not only from direct/contact-based bleed-off of electrical charges, but also due to noninvasive electromagnetic coupling (Figure 4). That is, as mentioned[11] in DOD-HDBK-263, electromagnetic pulses (EMP) caused by ESD in the form of a spark can cause part failures in equipment.

The following analysis will enable a simulation/modeling to represent such noninvasive ESD-base EMI threats. Consider an ESD event, say, from a finger tip occurring in the vicinity of a circular aperture on an equipment (shielding) as illustrated in Figure 5. For the purpose of analysis, the finger is regarded as a dielectric-wedge (vide the insert in Figure 5) inducing an intense electric field in the discharge gap. The propagating, transient electromagnetic field generated at the gap can be represented by the lightning function as follows:

$$e_1(t) = E_1[\exp(-At)-\exp(-Bt)] \qquad (1)$$

with A and B being constants dependent on the rise and decay times of the impulse discharge. The amplitude E_1 at the center of the discharge-gap is proportional[6] to $\tau\ D^{\tau-1}$ where D is the gap-width and τ is a parameter ($0<\tau<1$) dependent on the wedge-angle (α) and on the ratio of dielectric constants, $\varepsilon_2/\varepsilon_1$. The electric field E_1 becomes singular attaining infinitely large magnitude as D approaches zero. This enhanced local field (E_1) due to the wedge-like structure of the finger can be evaluated by the analysis due to Meixner.[12]

As the induced field is intercepted by the circular aperture on an (invariably) grounded and charge-free equipment-shield, the corresponding electromagnetic wave interior to the shielding is related to the exterior field components by means of a coupling coefficient (K) given by[13]

$$K = \frac{1}{\pi}\left[\theta_o - \frac{\sin\theta_o}{2} - \frac{\sin 2\theta_o}{2} - \frac{\sin 3\theta_o}{6}\right] \quad (2)$$

where θ_o is the semiangular width of the circular aperture, assumed to be located on a large, hollow, spherical shield (Figure 5) of radius, ρ.

The penetrated EMI is incident on a lossy dielectric sphere (of microscopic dimension) representing the vulnerable part ("hot-spot") in the microelectronic device, presumed to be located at the center of the spherical shield. The peak absorbed energy (W) at the dielectric sphere (with complex permittivity equal to $\varepsilon'-j\varepsilon''$) can be determined by the spherical wave expansion technique (Mie solution) due to Stratton[14] with appropriate boundary conditions and small argument approximations and by expressing the EMI field in the frequency domain through Fourier transform method. The result is,

$$W \simeq (4\pi a^3/3)\sigma K^2 E_1^2 \left|F(R,\theta,\phi)\right|^2 (B-A)^2/(B+A) \quad (3)$$

where $\sigma = \omega\varepsilon.\varepsilon''$ and,

$$\left|F(R,\theta,\phi)\right|^2 = [9/(\varepsilon'^2+\varepsilon''^2) + 0.4(k_o a/2)^2], \quad (4)$$

with k_o being the free-space propagation constant.

If A_J is the junction area in the device, $W/A_J\tau_o$ would refer to the average power density over a pulse duration, τ_o. Presuming that the failure occurs at t_d, the quantity $W/A_J\tau_o$ can be equated to the Wunsch-Bell's limit[15] of catastrophy (due to junction burnout) and the corresponding result yields an expression for the damage-time (t_d) as:

$$t_d = \tau_o^2 a_J^2 (T_m - T_i)^2 (\pi k_d \rho_o C_p)/W^2 \qquad (5)$$

where T_m and T_i are the melting point and initial temperature of the device, respectively; further, the quantities k_d, ρ_o and C_p, respectively, refer to thermal conductivity, density, and specific heat of the device material.

The results on damage-time (t_d) as a function of the rise-time (τ_r) of the excited transient field (Equation 1) indicate that the relative damage-time t_{d1}/t_{d2} (corresponding to two rise-times, namely, τ_{r1} and τ_{r2}) is approximately equal to $(\tau_{r1}/\tau_{r2})^2$ assuming that the pulse duration (τ_o) is constant and τ_r is equal to $\ell n(B/A)/(B-A)$. In the computation, the value of k_o was taken approximately equal to $2\pi/c\tau_r$ (with c being the free-space

velocity of the electromagnetic wave); further, the square-law relation between the relative values of t_d and τ_r is found to be valid, irrespective of the material of the device (that is, either silicon or GaAs).

The author has indicated elsewhere[16] that the relative damage-time directly specifies the lethality endurance coefficient (LEF) of the device. Hence, it follows from the present analysis that the LEF is equal to $(\tau_{r1}/\tau_{r2})^2$.

EXPERIMENTAL STUDIES

As radiated interference results from discharges to nearby conducting objects, the currents flowing through the conducting surface would create transient electromagnetic waves which can be picked up by wires acting as antennas interpreted as valid signals; or, the interference can also directly invade the devices causing catastrophic or latent failures. The extent of lethality is governed by the analysis indicated before.

The existence of ESD-based EMI can be verified by an experiment simulating the ESD-sparking environment. Per DOD-HDBK-263, ESD spark testing[11] can be performed by discharging the ESD in the form of a spark across a spark-gap sized for the ESD test voltage or by slowly bringing the high voltage test lead of the test circuit close to the case or electrical terminal of an ESD sensitive item while it is operating until the voltage is discharged in the form of an arc.

More elaborate test methods have been described by Honda and Ogura[17] who utilize time-domain and frequency-domain methods for quantitative prediction of ESD-based EMI.

Presently a simple arrangement is described to simulate the test studies under discussion. The principle of the test method is depicted in Figure 6, and Figure 7 illustrates the actual experimental set-up used.

A human-body zap simulator (IMCS Model 2600) is used to establish the spark across a metal tip and a grounded metal sheet. The simulator can provide positive or negative 25v to 25 kV peak, single or sequenced (5 or 10) pulses with variable ramp up rate of 5 to 25 kV/sec. The pulse mode operation corresponds to the human-body ESD of Figure 1.

The equipment/subassembly is simulated by portable static sensor (RITRC-1000) developed by the RIT Research Corporation. It is a miniaturized static sensor (originally developed to evaluate the efficacy of ESD protection bags) mounted on a PCB with an associated circuitry to respond with audio (buzzer) and video (LED) annunciations when the sensed static or static-induced electric field exceeds a present level.

The sensor was enclosed in an EMI shield (metallic sandwich box) with a small coupling hole of 1/4" diameter. It was placed at a convenient distance (d) from the induced spark, such that for a given discharge voltage (peak) V_s and ramp rate ($r=\frac{di_s}{dt}$) the sensor would annunciate the reception of

EMI. For a given gap width at the spark, it was observed that the sensor response level was proportional to product of V_s and r.

The test performed confirms the possible noninvasive interaction between an ESD and a nearby equipment via electromagnetic coupling; and quantitatively, such an interference is governed by the arc gap-width, coupling cross-section and the product of V_s and r.

CONCLUSIONS

From the analytical discussion presented before and from the experimental results obtained, the following conclusions can be inferred:

1. Quantification of EMI coupling reveals that the extent of severity involved primarily depends on the ESD source and the coupling through the shield.

2. The intrinsic lethality of the device is mainly a function of the electrothermal parameters of the junction in the vulnerable device.

3. The intensity and rise-time of the transient ESD overwhelmingly dictate the extrinsic-dependency of the device-lethality.

4. The present analysis also indicates that the influence of ESD via EMI is governed by the gap-width (D), as experimentally observed by Honda and Kawamura.[4]

5. The overall lethality of the device is directly proportional to the effective cross-section of the equipment exposed to the EMI, quantified via the coupling coefficient, K.

6. Intense EMI coupling would be experienced if the ESD event is provoked by short-tips or wedges.

7. The implicit dependency of device-lethality on the transient nature of the ESD (expressed in terms of τ_r) as evinced in the present work, concurs with the results due to Honda and Kawamura[4] who expressed the EMI severity in terms of the voltage and rate of change of current product ($V_s \times di_s/dt$) pertaining to the ESD loop (Figure 5).

8. Lastly, the relative lethality of the device to transient discharges is equal to the square of the relative rise-times of the transients.

There are two possible solutions against radiated interference from an ESD. The first method is simply to make the overall equipment shield as complete as possible. That is, making the shield a nearly seamless six-sided box, would reduce or eliminate the internal fields induced by the invading interference.

However, for cosmetic reasons, if a complete metal-housing is not possible, the second approach is to adopt second internal shields exclusive to ESD-sensitive PCBs and connect the second shield to the first (external shield) at the electrical power inlet. By this arrangement, the outer shield acts as radiating plane producing fields in its interior, the second shield, at the same time does not have induced current flowing through it. Similar effect can also be activated by a ground-plane under the PCB or multilayer board with a buried ground plane.

ACKNOWLEDGEMENT

This work was supported by a research grant from the Office of Naval Research (No. 613-005) which is gratefully acknowledged.

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CAPTIONS FOR THE DIAGRAMS

Figure 1: ESD: Human-Body Model

Figure 2: ESD: Charged-Device Model

Figure 3: ESD: Field-Induced Model

Figure 4: EMI Due to Static Effects

Figure 5: ESD-Based EMI: Modeling

Figure 6: Principle of Simulating ESD-Based EMI

Figure 7: ESD-Induced EMI Coupling To A Circuit: Experimental Set-Up

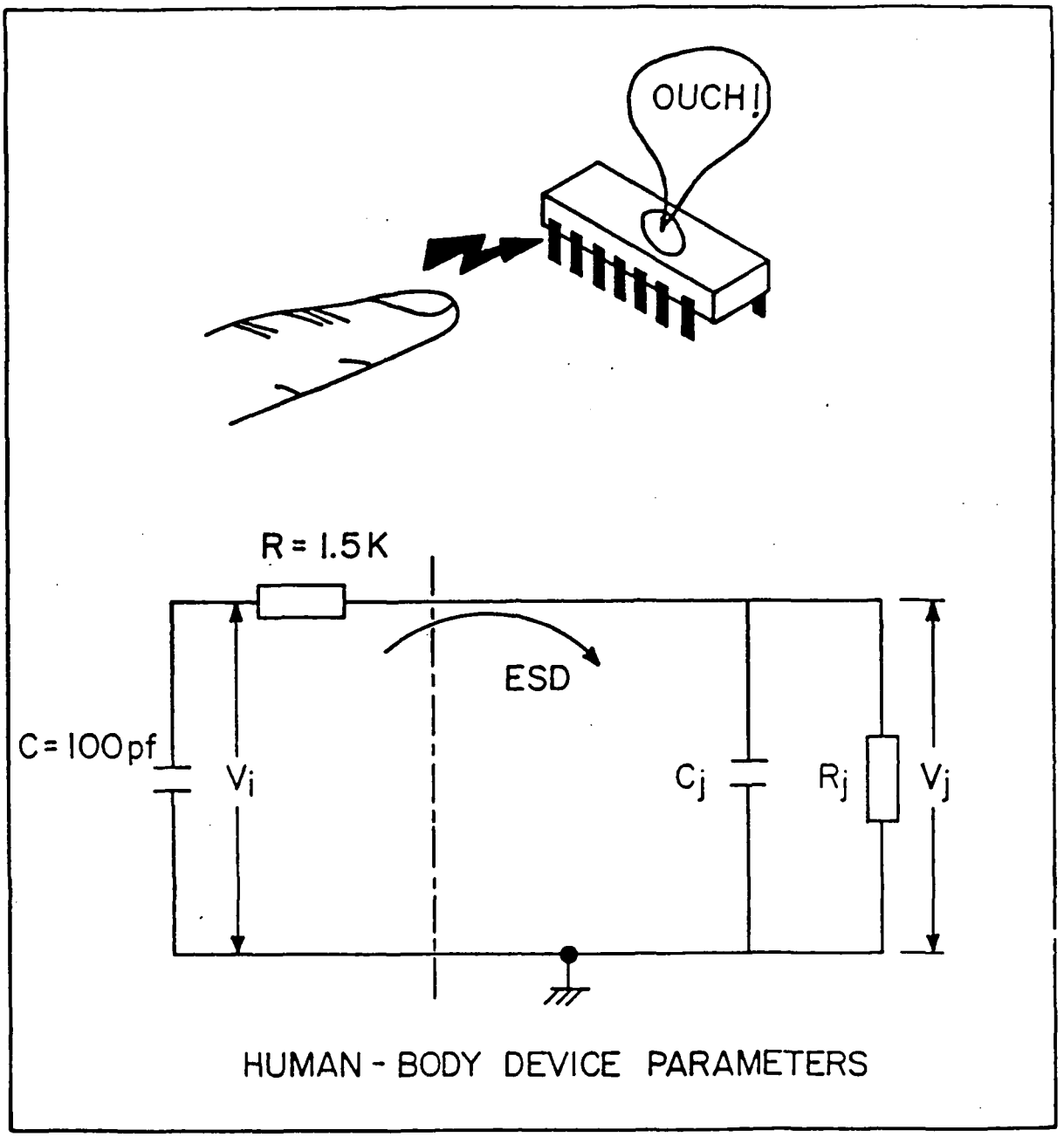


FIG. 1 ESD: HUMAN-BODY MODEL

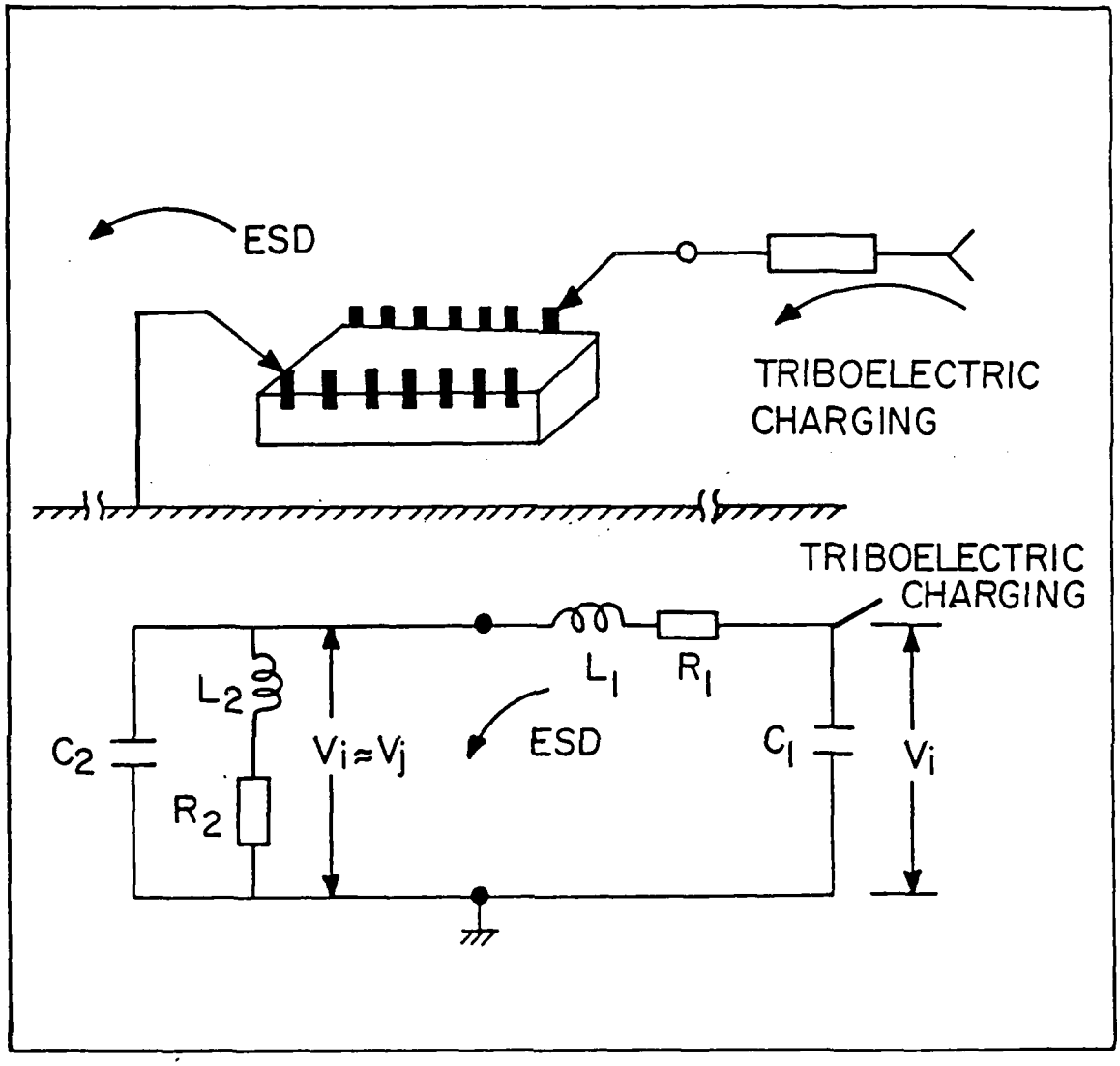


FIG. 2 ESD: CHARGED DEVICE MODEL

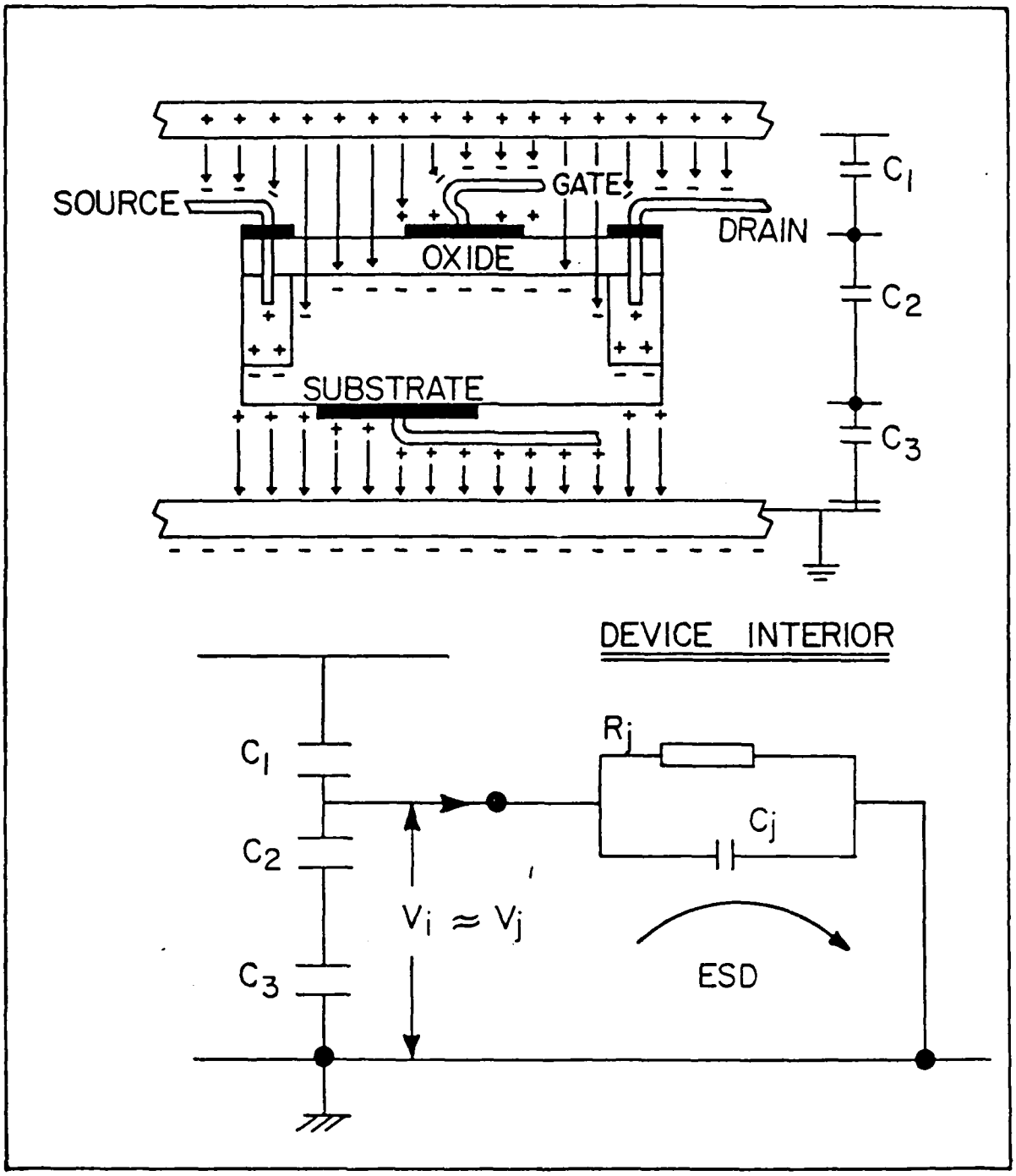


FIG.3 ESD: FIELD - INDUCED MODEL

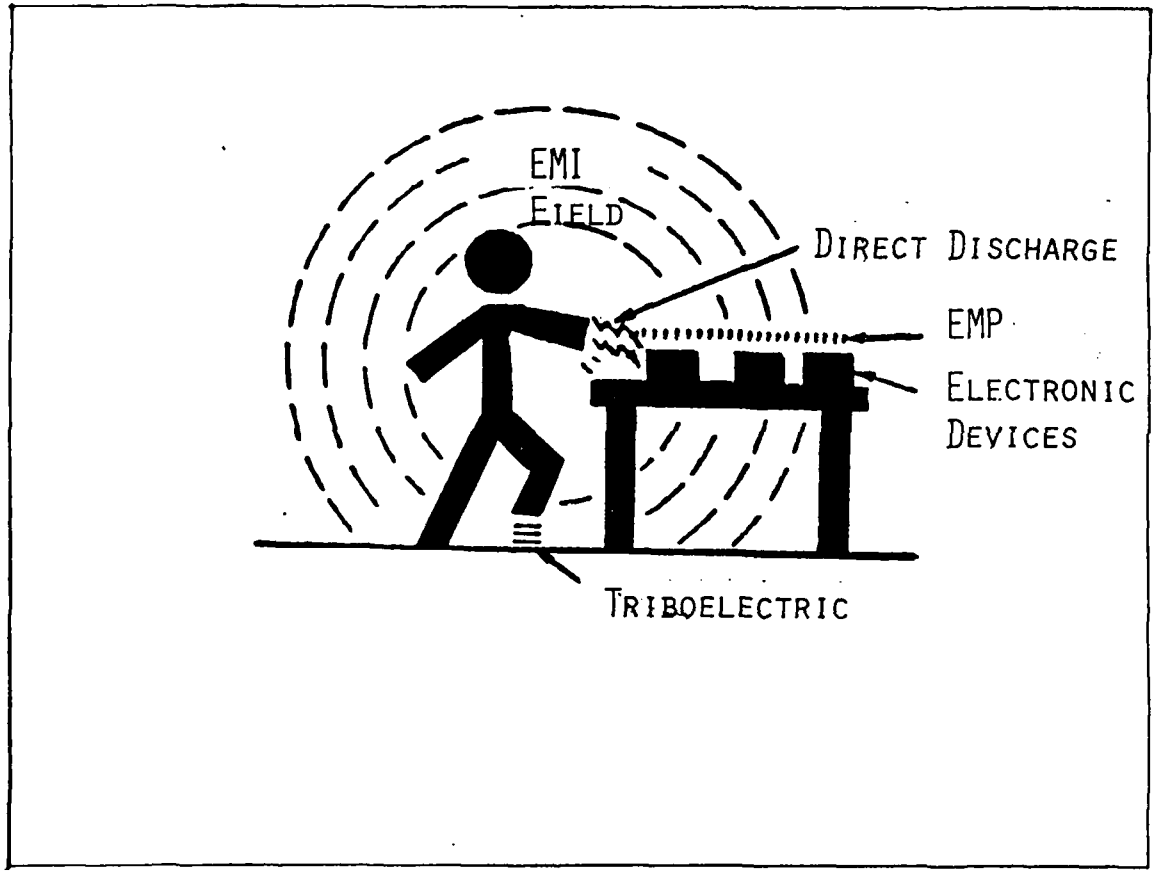


FIG. 4 EMI DUE TO STATIC EFFECTS

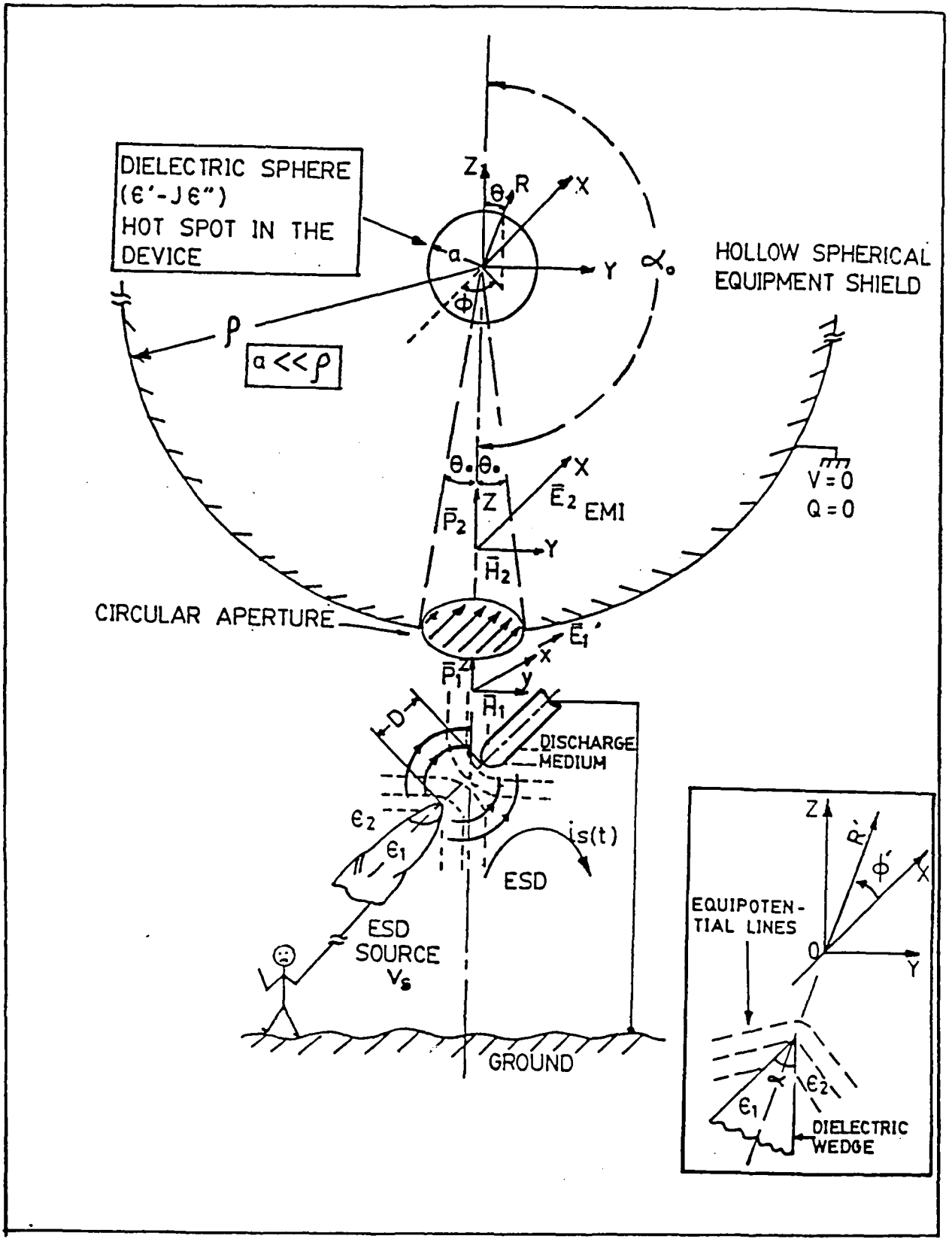


FIG. 5 ESD - BASED EMI: MODELING

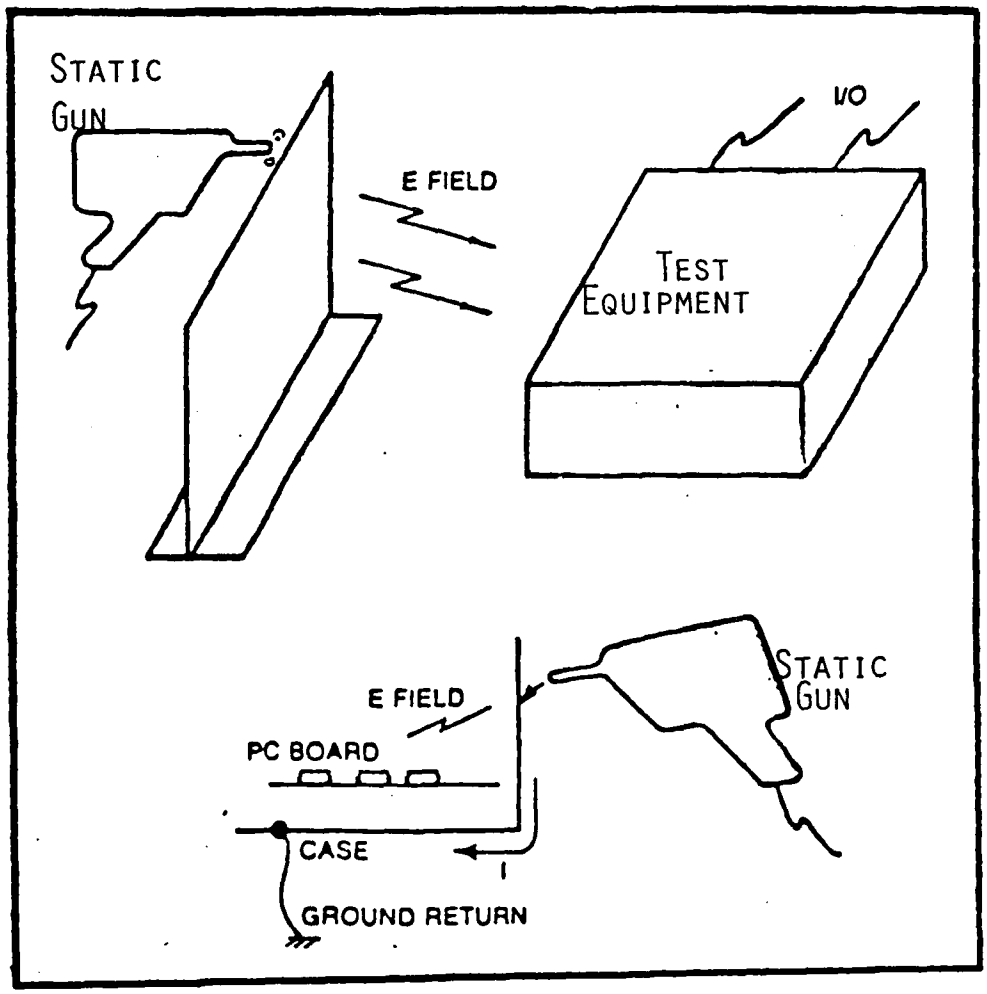


FIG. 6 PRINCIPLE OF SIMULATING ESD-BASED EMI

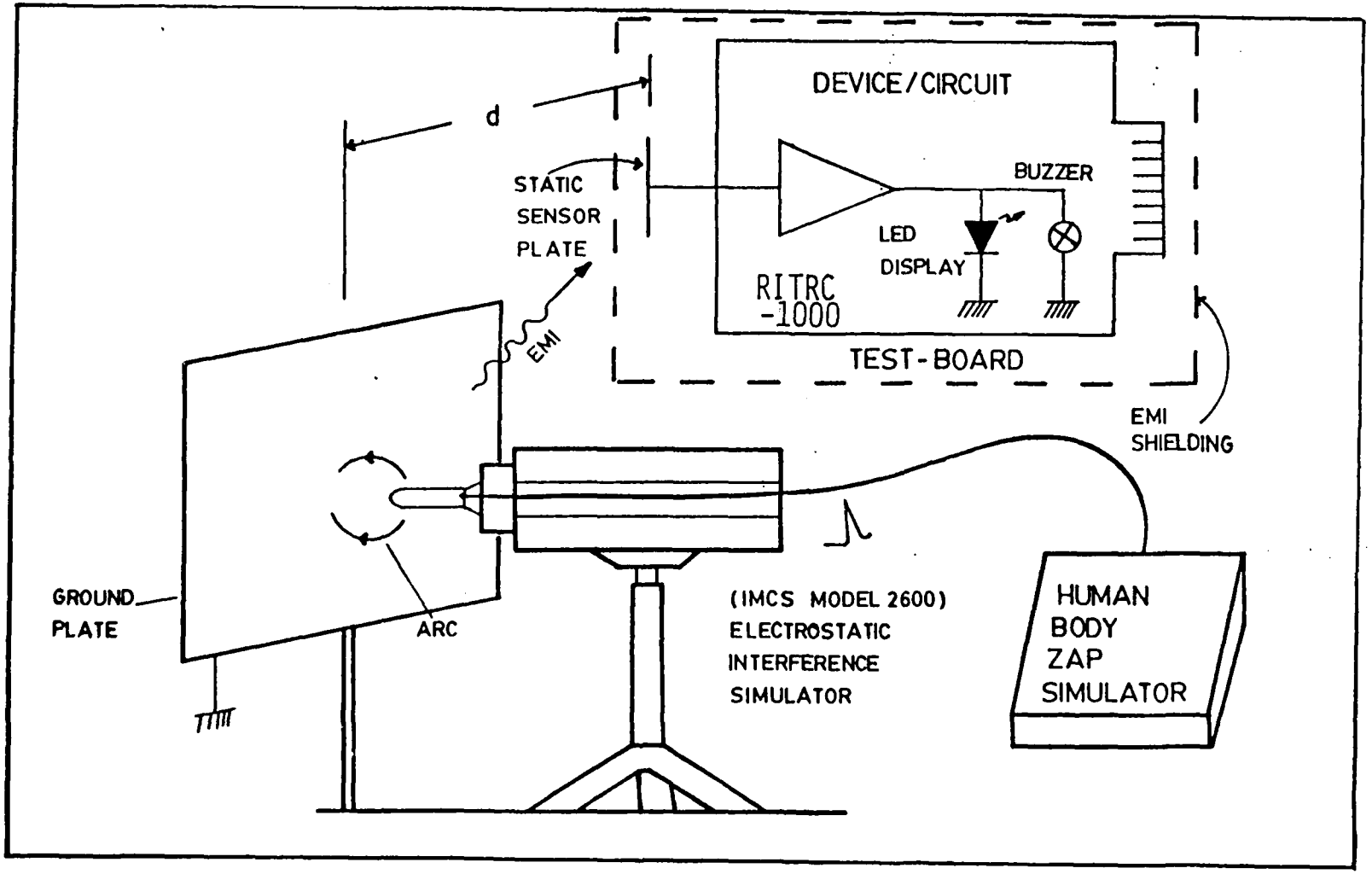


FIG. 7 **ESD** - INDUCED EMI COUPLING TO A CIRCUIT: EXPERIMENTAL SET-UP

IMPULSIVE EMI RADIATED BY ELECTROSTATIC DISCHARGES (ESD)

An understanding of failure of equipment-mounted devices due to indirect (noninvasive) energy transfer from the ESD via transient electromagnetic coupling/interference warrants a unique modeling.

Perambur S. Neelakantaswamy, RIT Research Corporation, Rochester, NY

INTRODUCTION

Conventional studies on ESD-based damages are usually restricted to chip-level.[1] However, an increased effort to investigate the susceptibility of equipment and subassemblies to ESD failures is now underway[2,3], because such larger systems expose prominent cross-sections to impulsive electromagnetic interference (EMI) emanating from an external ESD event.[4]. That is, equipment in general is potentially susceptible to accept electromagnetic waves radiated from an external ESD occurring in the vicinity. Therefore, any sensitive device mounted within the equipment is likely to be damaged by absorbing the interfering electromagnetic energy which penetrates through apertures (on the equipment-shielding) and/or is coupled via conductor surfaces, connectors, etc. Eventually, circuit malfunctioning and/or equipment breakdown can occur, depending on whether the failure is latent or catastrophic. The appearance of "ghost-bits" and "bit-dropouts" in computers and "sneaky" equipment failures in production lines, inspection departments, at the stockroom, while in-transit or in the field can be largely attributed to such ESD-based electromagnetic influences.[5]

To quantitatively evaluate the cause-effect relationship in the failure mode described above, it is essential to develop an EMI model representing the ESD-excited electromagnetic wave, its coupling to devices via equipment/subassembly cross-section(s) and the resulting damage. This article proposes a model to portray exclusively the implicit (EMI-based) ESD-to-device interaction in contrast with the existing models (human-body model[6], charged-model device[7], and field-induced model[8]) which rather describe the direct (contact-based) interactive damages.

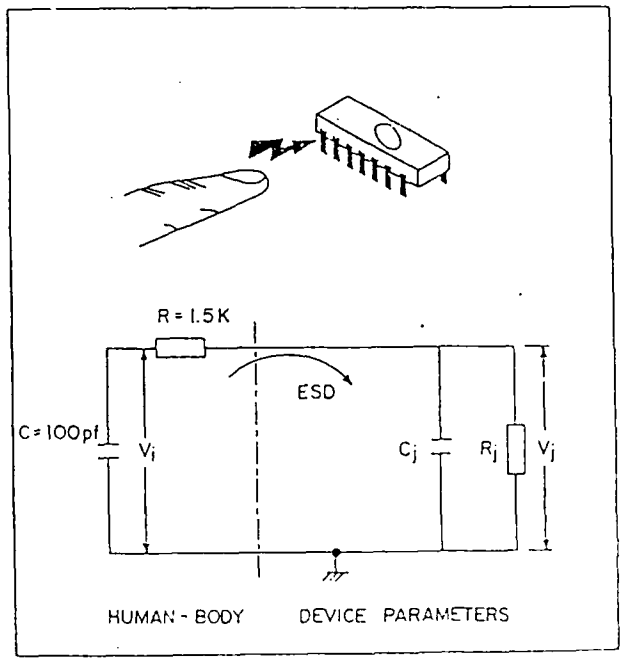


Figure 1. ESD: Human-Body Model.

ESD MODELS

The electrostatic discharge (ESD) phenomenon that plagues the modern electronics industry as a new contaminant is normally simulated by three well established models[6,7,8] describing the device to ESD interactions. The human-body model[6] shown in Figure 1 depicts the transfer of static from a charged person to ground via the test device. A charged-device model[7] (Figure 2) represents the bleed-off of accumulated charges (which otherwise "normally stay put as puddles" upon the device-surface) to ground through the pin(s) and/or conductive parts of the active device. The third model[8] simulates the effect of the charge distribution and discharge when a device is exposed to a static-electric field (Figure 3).

In general, ESD threats modeled as per Figures 1 to 3 are conceived and, supposedly, experienced only by isolated devices; that is, in those devices which are not subassembled or mounted on PCBs of the equipment. This presumption is somewhat incorrect, and as pointed out by Frank[9], it is a "myth" to presume "an ESD sensitive component cannot be damaged once it is installed on a circuit board." Notwithstanding, in the existing practice, the survivability assessment of electronic systems under electrical overstress (EOS) arising from ESD has been invariably restricted to an analysis of isolated components only and failure prevention measures have been prescribed accordingly — only to the handling and use of isolated devices. Further

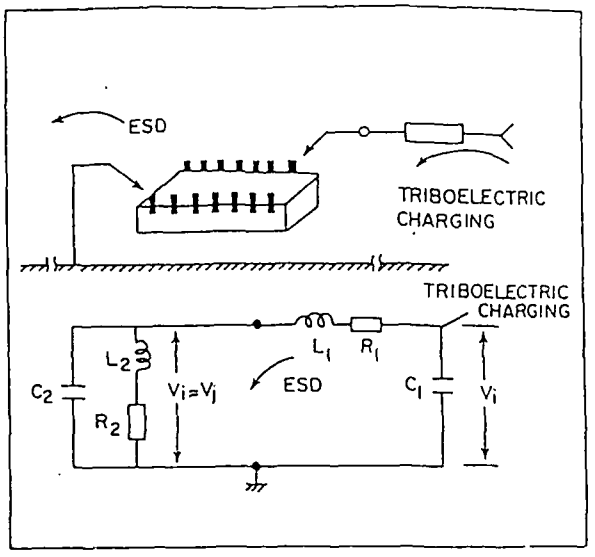


Figure 2. ESD: Charged-Device Model.

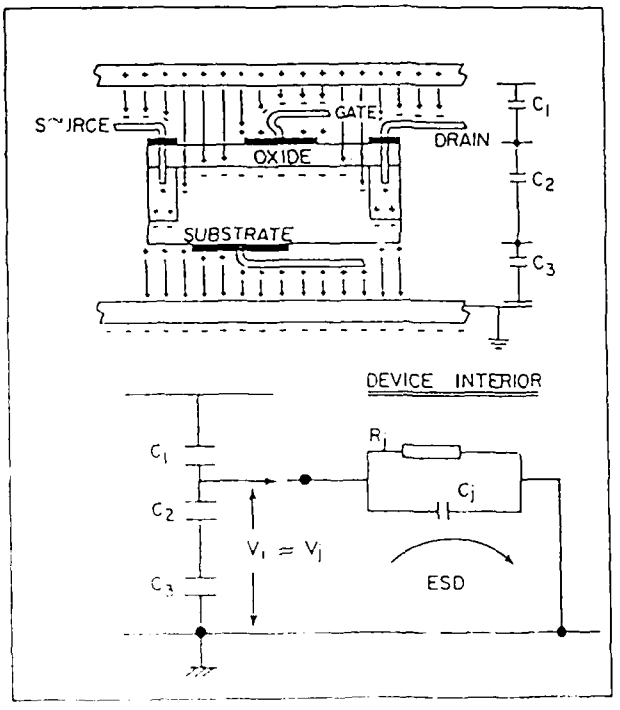


Figure 3. ESD: Field-Induced Model

failure threshold studies and protective circuit designs have been mostly based on anticipated ESD threats exclusive to unmounted/isolated devices.

However, case studies reveal that devices mounted on printed circuit boards (PCBs) in equipment would experience high failure rates under ESD environments despite exercising the prescribed precautionary measures. For example, as indicated by Thompson[2], non-observance of ESD-protective measures in handling and using certain costly replacement subassemblies of tactical systems, like missiles, resulted in excessive loss and warranted frequent field repairs.

Not taking care to protect ESD sensitive components from the damage after they have been installed in equipment can also result in performance degradation of the unit, as pointed out by Frank[9], referring to a case of a scientific calculator being unable to retain the programmed memory when necessary handling procedures were not followed.

More evidence on ESD-induced damage to integrated circuits on PCBs has recently been furnished by Shaw and Enoch[10] with experimental data pertaining to the sensitivity to ESD transients of a batch of octal-latch integrated circuits mounted on a printed circuit board. Their experiments reveal that the high static propensity of PCBs would lead to an ESD transient sufficiently large to cause catastrophic damage in mounted devices. Recently, the author has also studied[3] the susceptibility of PCB-mounted devices to failures caused by ESD and indicated the higher vulnerability of subassembled structures.

EMI MODEL

In ESD problems related to subassembled and/or equipment-mounted devices, the threat would arise not only from direct/contact-based bleed-off of electrical charges, but from noninvasive electromagnetic coupling as well (Figure 4). That is, as mentioned[11] in DOD-HDBK-263, electromagnetic pulses (EMP) caused by ESD in the form of a spark can cause part failures in equipment.

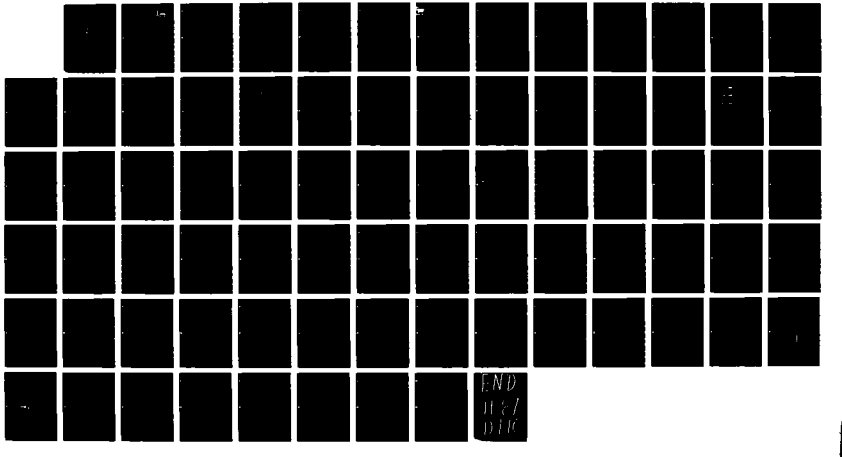
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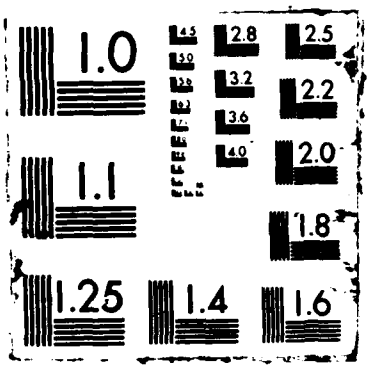
$$e_1(t) = E_1[\exp(-At) - \exp(-Bt)]$$

with A and B being [illegible] dent on the rise and [illegible] the impulse discharge [illegible] tude E_1 at the [illegible] charge-gap is [illegible] where D is the [illegible] parameter [illegible]

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the wedge-angle (α) and on the ratio of dielectric constants, ϵ_2/ϵ_1. The electric field E_1 becomes singular attaining infinitely large magnitude as D approaches zero. This enhanced local field (E_1) due to the wedge-like structure of the finger can be evaluated by the Meixner analysis.[12]

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$$K = 1/\pi(\theta_o - (\sin\theta_o)/2 - (\sin 2\theta_o)/2 + (\sin 3\theta_o/6) \quad (2)$$

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where $\sigma = \omega\epsilon.\epsilon'$ and,

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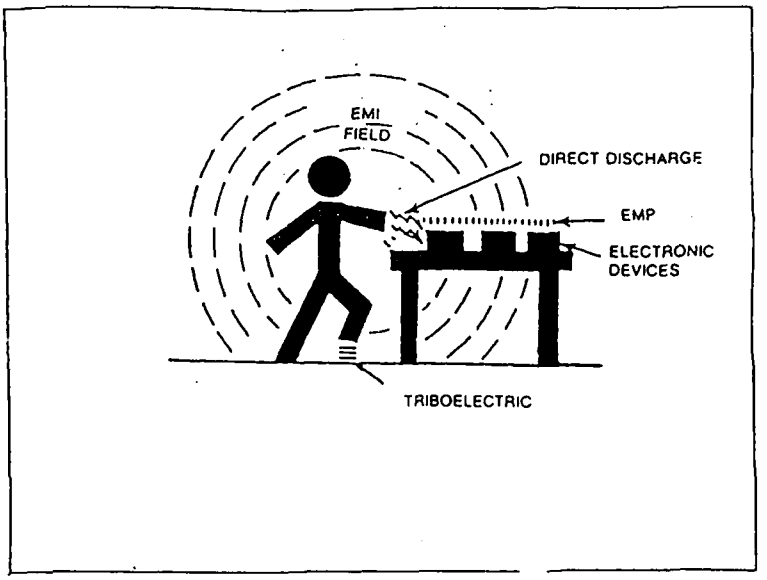


Figure 4. EMI Due to Static Effects.

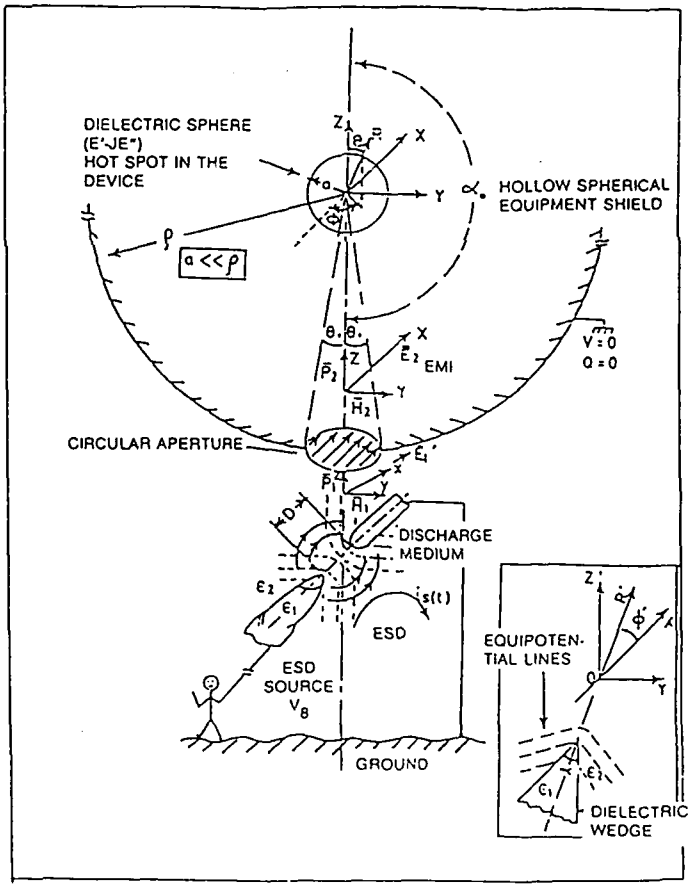


Figure 5. ESD-Based EMI: Modeling.

where T_m and T_i are the melting point and initial temperature of the device, respectively; further, the quantities k_d, ρ_o and C_p, refer to thermal conductivity, density, and specific heat of the device material, respectively.

The results on damage-time (t_d) as a function of the rise time (τ_r) of the excited transient field (Equation 1) indicate that the relative damage-time t_{d1}/t_{d2} (corresponding to two rise times, namely, τ_{r1} and τ_{r2}) is approximately equal to $(\tau_{r1}/\tau_{r2})^2$ assuming that the pulse duration (τ_o is constant and τ_{or} is equal to $\log_e(B/A)/(B-A)$. In the computation, the value of k_0 was taken approximately equal to $2\pi/c\tau_r$ (with c being the free-space velocity of the electromagnetic wave); further, the square-law relation between the relative values of t_d and τ_r is found to be valid, irrespective of the material of the device (i.e., either silicon or GaAs).

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EXPERIMENTAL STUDIES

As radiated interference results from discharges to nearby conducting objects, the currents flowing through the conducting surface create transient electromagnetic waves which can be picked up and interpreted as valid signals by wires acting as antennas; or, the interference can directly invade the devices causing catastrophic or latent failures. The extent of lethality is governed by the analysis previously indicated.

The existence of ESD-based EMI can be verified by an experiment simulating the ESD-sparking environment. ESD spark testing[11], per DOD-HDBK-263, can be performed by discharging the ESD in the form of a spark across a spark-gap sized for the ESD test voltage or by slowly bringing the high voltage test lead of the test circuit close to the case or electrical terminal of an operating ESD-sensitive item until the voltage is discharged in the form of an arc.

More elaborate test methods have been described by Honda and Ogura[17] who utilize time-domain and frequency-domain methods for quantitative prediction of ESD-based EMI.

A simple arrangement, depicted in Figure 6 and Figure 7, is described to simulate the test studies under discussion. A human-body zap simulator is used to establish the spark across a metal tip and a grounded metal sheet. The simulator can provide positive or negative 25 V to 25 kV peak, single or sequenced (5 or 10) pulses with variable ramp-up rate of 5 to 25 kV/sec. The pulse mode operation corresponds to the human-body ESD of Figure 1.

The equipment/subassembly is simulated by a portable, miniaturized static sensor (originally developed to evaluate the efficacy of ESD-protection bags) mounted on a PCB with an associated circuitry to respond with audio (buzzer) and video (LED) annunications when the sensed static or static-induced electric field exceeds a present level. The sensor was enclosed in an EMI shield (metallic sandwich box) with a small coupling hole of ¼-inch diameter. It was placed at a convenient distance (d) from the induced spark, such that for a given discharge voltage (peak) V_s and ramp rate ($r = di_s/dt$) the sensor would annunciate the reception of

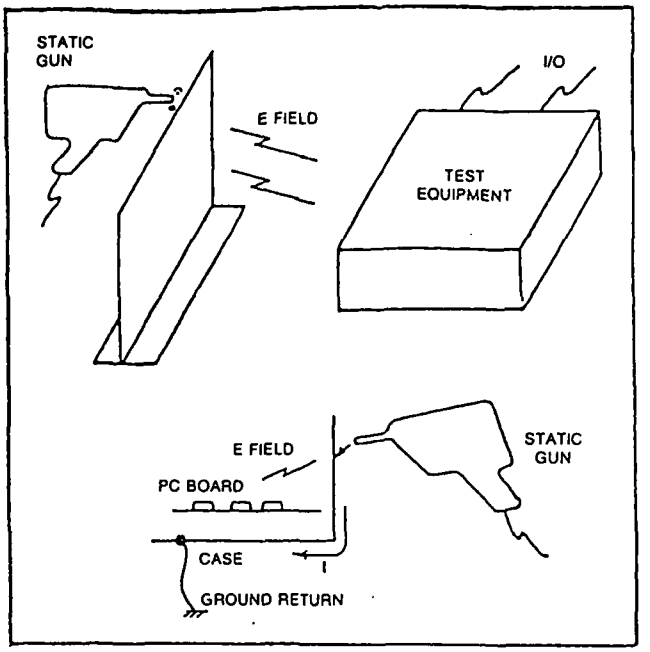


Figure 6. Principle of Simulating ESD-Based EMI.

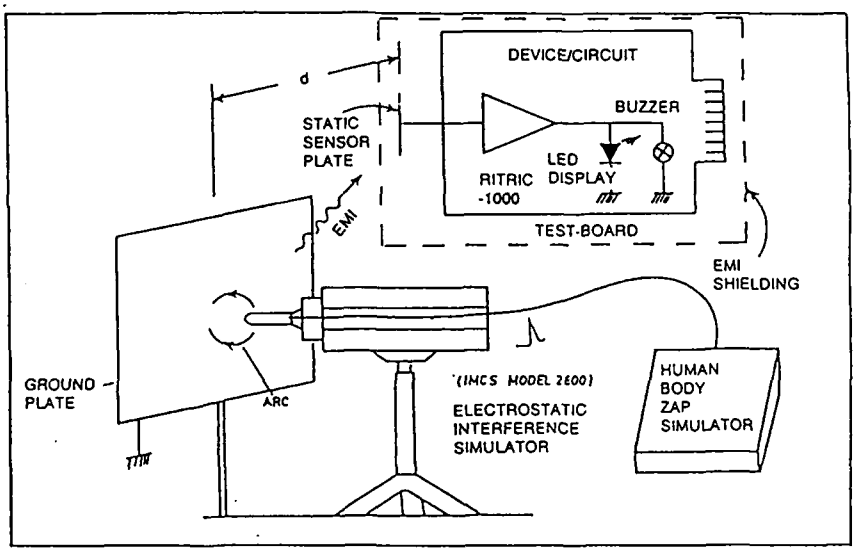


Figure 7. ESD-Induced EMI Coupling to a Circuit: Experimental Setup.

EMI. For a given zap width at the spark, it was observed that the sensor response level was proportional to the product of V_s and r.

The test performed confirms the possible noninvasive interaction between an ESD and nearby equipment via electromagnetic coupling, and that quantitatively, such an interference is governed by the arc gap-width, coupling cross-section and the products of V_s and r.

CONCLUSIONS

From the analytical discussion previously presented and from the experimental results obtained, the following conclusions can be inferred:

1. Quantification of EMI coupling reveals that the extent of severity involved primarily depends on the ESD source and the coupling through the shield.
2. The intrinsic lethality of the device is mainly a function of the electrothermal parameters of the junction in the vulnerable device.
3. The intensity and rise time of the transient ESD overwhelmingly dictate the extrinsic dependency of the device-lethality.
4. The present analysis also indicates that the influence of ESD via EMI is governed by the gap-wdth (D), as experimentally observed by Honda and Kawamura[4].
5. The overall lethality of the device is directly proportional to the effective cross-section of the equipment exposed to the EMI, quantified via the coupling coefficient, K.
6. Intense EMI coupling would be experienced if the ESD event is provoked by short-tips or wedges.
7. The implicit dependency of device-lethality on the transient nature of the ESD (expressed in terms of τ_r) as evinced in the present work, concurs with the results of Honda and Kawamura[4] who expressed the EMI severity in terms of the voltage and rate of change of current product ($V_s \times di_s/dt$) pertaining to the ESD loop (Figure 5).
8. Lastly, the relative lethality of the device to transient discharges is equal to the square of the relative rise times of the transients.

There are two possible solutions against radiated interference from an ESD. The first method is simply to make the overall equipment shield as complete as possible. That is, making the shield a nearly seamless six-sided box would reduce or eliminate the internal fields induced by the invading interference.

However, for cosmetic reasons, if a complete metal housing is not possible, the second approach is to adopt second internal shields exclusive to ESD-sensitive PCBs and connect the second shield to the first (external shield) at the electrical power inlet. By this arrangement, the outer shield acts as a radiating plane producing fields in its interior. The second shield, at the same time, does not have induced current flowing through it. A similar effect also can be activated by a ground plane under the PCB or multilayer board with a buried ground plane.

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The endochronic degradation of MOS devices arising from the global response of the device parameters collectively deteriorating under the repetitive influence of electrical overstresses (at subcatastrophic levels) such as electrostatic discharge (ESD), electromagnetic pulsing (EMP), etc., is quantified in terms of noise characteristics. Life-time studies depicting the degradation of a test device are presented. Computed and experimental data are furnished.

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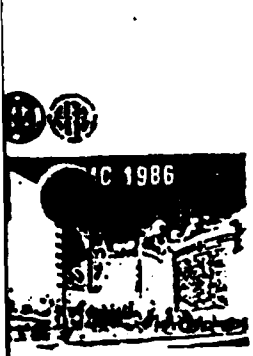
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NOISE CHARACTERISTICS OF MOS DEVICES

DEGRADED BY

ELECTRICAL OVERSTRESSES



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NOISE PERFORMANCE STUDIES TO ASSESS MOS-DEVICE DEGRADATION DUE TO IMPULSIVE OVERSTRESSES

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ABSTRACT

The endochronic degradation of MOS devices arising from the global response of the device parameters collectively deteriorating under the repetitive influence of electrical overstresses (at subcatastrophic levels) such as electrostatic discharge (ESD), electromagnetic pulsing (EMP), etc., is quantified in terms of noise characteristics. Life-time studies depicting the degradation of a test device are presented. Computed and experimental data are furnished.

INTRODUCTION

Studies on gate-oxide degradation of electrically overstressed MOS devices subjected to ESD/EMP environments are useful to establish design-reviews required to achieve reduced device instabilities and improved performance reliability.

The effect of electrical-overstressing of gate-oxides primarily causes charge-trapping in the oxide-region together with the corresponding changes in the interface states.[1] In general, intensity, polarity and the rate of occurance of overstressing voltages would determine the extent of damage to the insulator integrity.[2] While high-level zaps would cause oxide puncture(s) with catastrophic (irreversible) damages, subcatastrophic transients occuring repeatedly may cause a cumulative growth of device degradation and the time-dependent or endochronic damage of the device would be reflected in measurable parameters,[3] such as transconductance (g_m), threshold voltage (V_t), etc. Inasmuch as all the degrading device parameters are interdependent, the cohesive damage of the device should be assessed by an appropriate characteristic function which collectively represents the net physical damage due to overstressings. It is presently demonstrated that noise characteristics can depict the global representation of the stochastical variations in charge-trapping and interface generation under external overstressings; and noise measurements of degraded devices can therefore be useful for accelerated test procedures adopted in life-time modeling strategies.

THEORETICAL CONSIDERATIONS

The ESD phenomena normally encountered can be simulated by three well-established models, namely,[4] (a) human-body model, (b) charged-device model, and (c) field-induced model. The human-body model (Fig. 1) depicts the transfer of static from a charged individual to ground via the test device.

Charged-device[5] model represents the bleed-off of accumulated charge upon the device-surface to ground through the pin and conductive parts of the active device (Fig. 2). The third model simulates the effect of the charge distribution and discharge when a device is exposed to a static-electric field (Fig. 3).

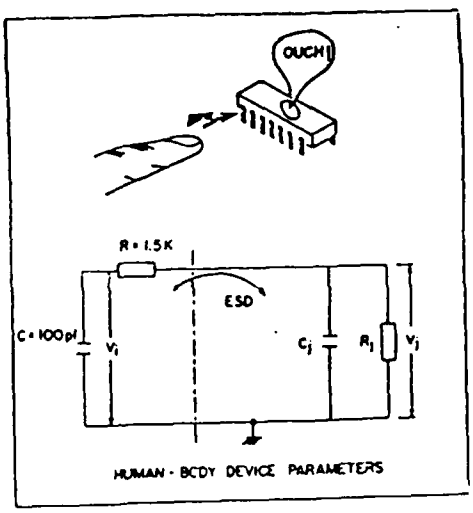


FIG 1 HUMAN – BODY MODEL

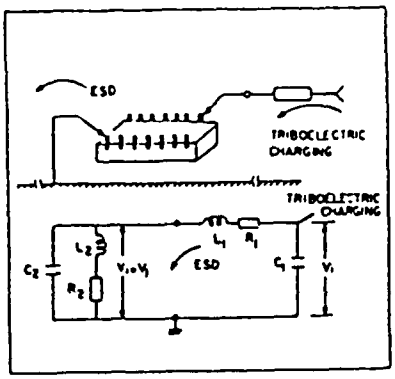


FIG 2 CHARGED-DEVICE MODEL

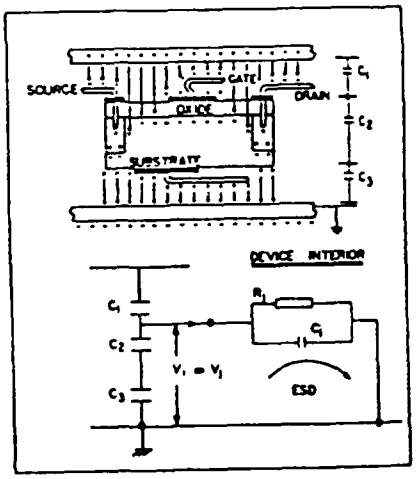


FIG 3: FIELD-INDUCED MODEL

When a MOS device is subjected to an electrical overstressing at the gate due to an impulsive transient caused by an ESD (or an EMP), the corresponding induction of charge-trapping and generation of interface states can be equivalently represented by an input noise resistence R_N given by[6]

$$R_N = \left(\frac{N_s}{4kT}\right)\left(\frac{qt_{ox}}{\varepsilon_{ox}}\right)^2\left(\frac{\mu_s}{\mu_o}\right)^2 \qquad (1)$$

where k is the Boltzmann constant, T is the temperature (~300 K) and q is the electronic charge. Further, t_{ox} and ε_{ox} are the thickness and the permittivity of the gate-oxide, respectively; N_s is the surface-state density and μ_s/μ_o refers to the field-effect mobility to low field-mobility ratio.

Eq. (1) indicates that R_N is directly proportional to N_s concurring with the experimental results due to Abovitz[7] et al (Fig. 4). Hence the time-dependent history of N_s as controlled by any external overstressings can be tracked via the assessment of R_N.

The field-effect mobility is also dependent on N_s and is therefore linked[3,8] with the device parameters g_m and V_t. Explicitly,

$$\frac{\mu_s}{\mu_o} = \frac{1}{1+\alpha N_s} = \frac{g_m}{g_{mo}} = \frac{1}{1+\beta(V_G-V_t)} \qquad (2)$$

Here α and β are constants and g_{mo} refers to the value of g_m under unstressed conditions. Further, V_G is the applied gate potential.

From Eq. (1) and (2), the following relation can be obtained:

$$\frac{\Delta R_N}{R_N} = \frac{\Delta g_m}{g_m}\left[2 - \frac{1}{1-\frac{\Delta V_t}{\beta V_t}\,(V_G-V_T)}\right] \qquad (3)$$

The constant β has the approximate values of 0.138 and 0.308 for the n-channel and p-channel MOSFETs, respectively.[8]

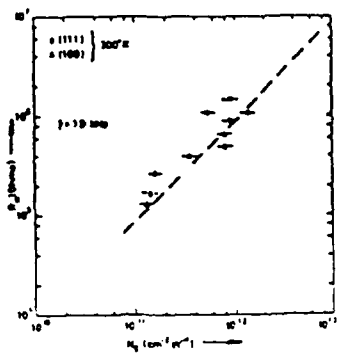


FIG 4 SURFACE STATE DENSITY VERSUS NOISE RESISTANCE: MOS DEVICE (REF 7)

EXPERIMENTAL STUDIES

A typical n-channel (enhancement mode) MOSFET was subjected to subcatastrophic zaps at its gate-input using a human-body ESD simulator (Fig. 1). Variations of g_m and V_t were measured as the functions of the number of zaps. Fig. 5 illustrates the relevant results.

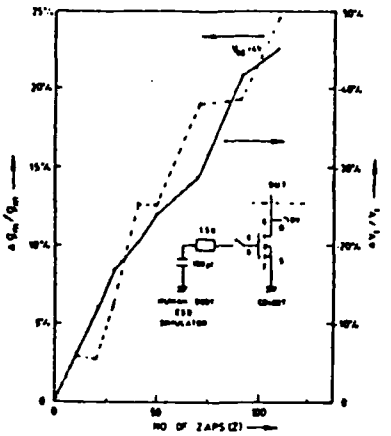


FIG 5 VARIATION OF g_m & V_t WITH RESPECT TO NUMBER OF ZAPS

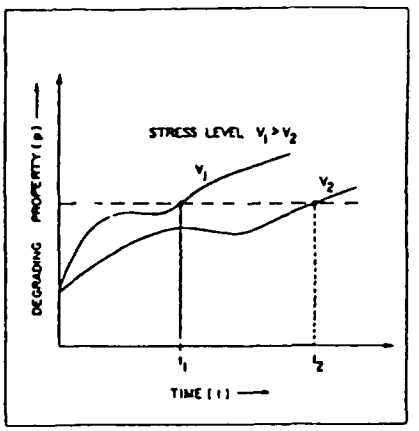


FIG.7 DEGRADATION VERSUS TIME UNDER TWO DISTINCT STRESS LEVELS

NOISE PARAMETER VESUS AGING

Using the results presented in Fig. 5, the fractional change in R_N as a function of the number of zaps (Z) can be calculated via Eq. (3). Thus Fig. 6 depicts the relevant computed data shoving that the rate of variation of R_N is approximately twice as that of g_m. Further, $\Delta R_N/R_N$ is linearly proportional to Z confirming the observations of Abovitz, et al.[7] Hence, the present study indicates the plausibility of assessing the EOS-based degradation via noise characterization.

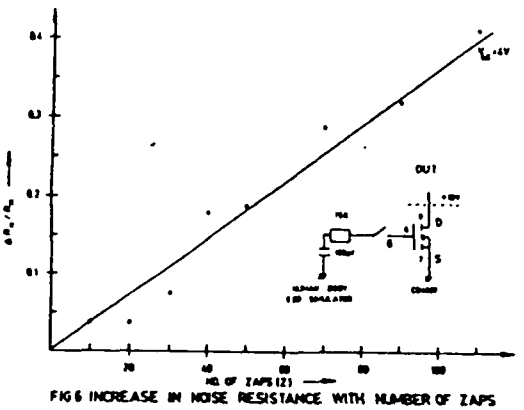


FIG 6 INCREASE IN NOISE RESISTANCE WITH NUMBER OF ZAPS

AGING MODEL

Cumulative build-up of degradation with the recurrence of zaps amounts to a dormant stage of failure during vhich the device vould exhibit a performance degradation leading to out-of-spec condition(s). This device-aging can be assessed by measuring the time variation of a nondestructive property (p) such as a noise parameter as indicated in the present analysis. Suppose two time-variation curves are obtained corresponding to two distinct (subcatastrophic) stress-levels. The functional form of p will be independent of the stress magnitude and the two curves will have the same shape, but different length (along the time axis) as shovn in Fig. 7. The times corresponding to same (extent of) aging under two distinct stress levels can be denoted as t_1 and t_2 (Fig. 7) and are known as "equivalent times."[9] By the application of "equivalent aging principle," it is possible to relate the equivalent times in terms of their corresponding stress levels, namely, V_1 and V_2. It is given by[9]

$$V_1^n \; t_1 = V_2^n \; t_2 = K_1 \text{ (Constant)} \qquad (4)$$

vhere n is the endurance coefficient. Eq. 4 can also be vritten in terms of the average numbers of zaps Z_1 and Z_2 occurred during the period t_1 and t_2, respectively. That is,

$$V_1^n \; Z_1 = V_2^n \; Z_2 = K_2 \text{ (Constant)} \qquad (5)$$

Thus, from Eq. 4 or 5, for a given severity level, the corresponding value of failure-time (or average number zaps during the period of failure-time) can be assessed by determining the values of n and K.

Further, the device reliability relevant to the endochronic degradation can be modeled by assuming that degradation rate is proportional to the existing degradation.[10] The proportionality constant is a positively distributed random variable and the extent of degradation would tend to be asymptotically log-normal. Hence the general form of life distribution Z (number of zaps) is given by

$$G(Z,p_c) = 1-\phi\left[\frac{\ln(p_c)-\mu}{\sigma}\right] \qquad (6)$$

where ϕ is the standard normal distribution and $p_c = r - r_c$. Here $r = \Delta R_N/R_N$ and the suffix c depicts the critical value of r. Further ln (p_c) has a mean value of and a standard deviation of σ. This log-normal aspect of life-time statistics as applied to endocronic degradation has been verified by the authors (with the MOS input leakage current as the control parameter, p) and the results are presented elsevhere.[11]

CONCLUSIONS

From the results presented here, the following conclusions can be inferred:

1. Noise parameter changes in a MOS device subjected to electrical overstressings represent the global, time-dependent degradation.

2. Such noise parameter variation expressed in terms of the fractional change in the noise resistance (R_N), is explicitly related to two major MOS-device parameters, namely, g_m and V_t (Eq. 3).

3. The rate of change of R_N with respect to the number of zaps is approximately linear.

4. Further, this rate of change of R_N is approximately twice the corresponding change in g_m.

5. Using $\Delta R_N/R_N$ as a control parameter (p), the principle of equivalent aging can be applied to MOS degradation for accelerated aging studies.

6. The degradation process can be modeled with log-normal distribution for relevant lifetime statistical analysis.

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Conference Record of 1986 IEEE International Symposium on Electrical Insulation, Washington, DC, June 9-11, 1986

GATE-INSULATOR DEGRADATION IN MOS-DEVICES DUE TO ELECTRICAL OVERSTRESSINGS: CHARACTERIZATION VIA NOISE PERFORMANCE STUDIES

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ABSTRACT - Design-reviews required to achieve improved performance reliability warrant the assessment of gate-insulator degradation in metal-oxide semiconductors (MOS) subjected to electrical overstressing (EOS) environments involving electrostatic discharges (ESD) and/or electromagnetic pulsing (EMP). The collective response of all the degrading parameters of the stressed devices can be cohesively studied via noise performance characteristics, as indicated in the present analysis. The global influence of overstressing quantified in terms of degrading noise parameters is useful in life-time prediction efforts. Relevant test calculations and experimental data are presented.

INTRODUCTION

Assessment of gate-insulator degradation in metal-oxide semiconductor (MOS) devices caused by electrical overstresses (EOS), such as electrostatic discharge (ESD), electromagnetic pulsing (EMP), etc., is essential for necessary design-reviews required to achieve reduced device-instabilities and improved performance reliability.

The primary effect of electrical overstressing is to cause a charge-trapping phenomenon in the gate-oxide film [1]. The extent of gate-oxide degradation arising from electrical overstressing would depend on the cumulative magnitude of charge-trapping and the corresponding changes in the interface-states; and hence, it is directly dependent on the intensity and rate of occurrence of electrical overstressings.

In the existing studies [1,2] on gate-oxide degradation, the parameters normally considered to characterize the influence of overstressing and the resulting charge-trapping/surface-state effects are [3], (a) device transconductance, g_m; (b) gate-current due to pumped-in charges, I_{cp}; (c) gate-oxide capacitance, C_{ox}; and (d) threshold voltage, V_t. Inasmuch as the aforesaid parameters are largely interdependent, the estimation of one of these parameters (to depict the degradation) as a function of overstressing does not explicitly account for the deviatory characteristics of the rest of the parameters.

Hence, it is purported in the present investigations to develop a new and cohesive formulation in terms of noise performance of the MOS device to characterize the overall degradation due to overstressing. The noise characteristics of a MOS device would, in general, depict the collective response of all the degrading parameters. This is because the net effects of charge-trapping and the associated occupation of surface states can be viewed as random/fluctuating phenomena which manifest as the device-noise with a typical 1/f type power-spectrum. That is, noise characterization would present the global influence of overstressing unlike the other parameters (specified earlier) which would rather represent the partial effects only.

In the present studies, an analytical formulation relating the charge-trapping and the electrical overstressing is derived in terms of an equivalent noise resistance. Measured data acquired from a typical MOS integrated circuit subjected to electrical overstressings are presented.

ANALYSIS

The ESD phenomena normally encountered can be simulated by three well-known models, namely, (a) human-body model [4], (b) charged-device model [5], and (c) field-induced model [6]. The human-body model (Fig. 1) depicts the transfer of static from a charged individual to ground via the test device. Charged device model represents the bleed-off of accumulated charge upon the device-surface to ground through the pin(s) and conductive parts of the active device (Fig. 2). The third model simulates the effect of the charge distribution and discharge when a device is exposed to static electric field (Fig. 3).

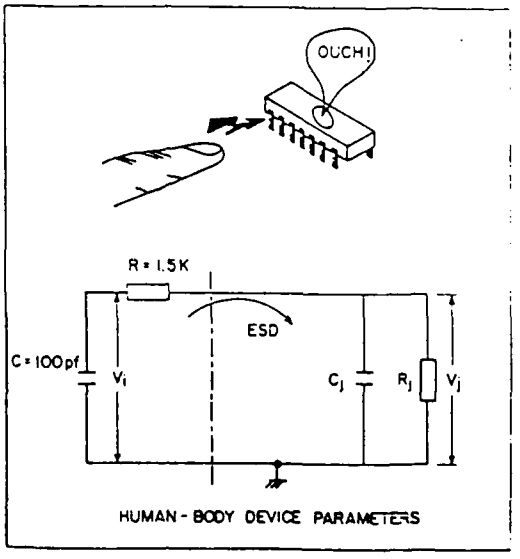


FIG 1 : HUMAN - BODY MODEL

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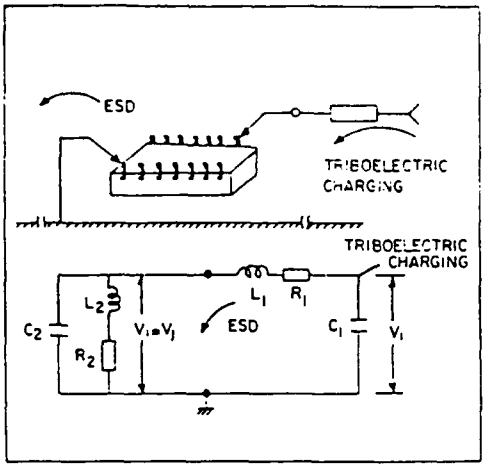


FIG 2 . CHARGED-DEVICE MODEL

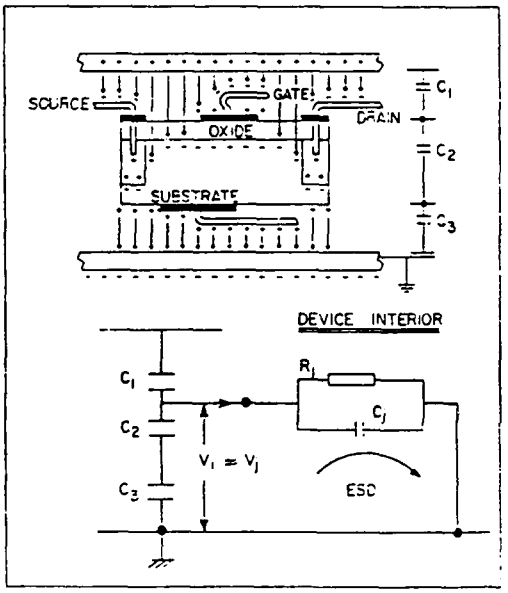


FIG 3 FIELD-INDUCED MODEL

When a MOS device is subjected to electrical overstressings at the gate due to impulsive transients caused by electrostatic discharges (ESD), the corresponding induction of charge-trapping and generation of interface-states can be specified in terms of the stochastical aspects of charge-accumulation represented by the device noise characteristics. Than is, under identical pumped-in current by repetitive transients, Leventhal [6] has shown that the resulting input noise resistance R_N is given by

$$R_N \propto \left(\frac{1}{4kT}\right)\left(\frac{qt_{ox}}{\varepsilon_{ox}}\right)\left(\frac{N_s\mu_s^2}{\mu_o^2}\right) \qquad (1)$$

where k is the Boltzman constant, T is the temperature (~ 300 K) and q is the electronic charge. Further, t_{ox} and ε_{ox} are the thickness and permittivity of the gate-oxide, respectively; N_s is the surface-state density and μ_s/μ_o refers to the field-effect mobility to low-field mobility-ratio.

Eqn. (1) indicates that R_N is directly proportional to N_s concurring with the experimental results due to Abovitz, et al [7], (Fig. 4). Hence the endochronic history of N_s as dictated by external overstressings can be tracked via noise parameter measurements.

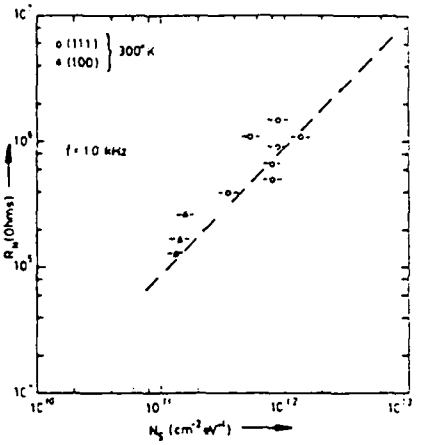


FIG 4 SURFACE STATE DENSITY VERSUS NOISE RESISTANCE: MOS DEVICE (REF. 7)

The field-effect mobility is itself dependent on N_s as well as on the other device parameters, namely, the transconductance (g_m) and the threshold voltage (V_t). Explicitly, by using the results of Hsu and Tam [3] and Akers, et al [8], one obtains

$$\frac{\mu_s}{\mu_o} = \frac{1}{1+\alpha N_s} = \frac{g_m}{g_{mo}} = \frac{1}{1+\beta(V_g - V_t)} \qquad (2)$$

where α and β are constants and g_{mo} refers to g_m under unstressed conditions. Further, V_g is the applied gate potentials.

Combining Eqs. (1) and (2), the following relation is obtained for the fractional values of R_N, V_t and g_m.

$$\frac{\Delta R_N}{R_N} \propto \frac{\Delta g_m}{g_{mi}}\left[2 - \frac{1}{1 - \frac{\Delta V_t}{(V_g - V_t)}}\right] \qquad (3)$$

EXPERIMENTAL STUDIES

A typical n-channel (enhancement mode) MOSFET was subjected to subcatastrophic zaps at its gate-input using a human-body simulator (Fig. 1). Variations of g_m and V_t measured as the functions of the number of zaps. Fig. 5 illustrates the relevant results.

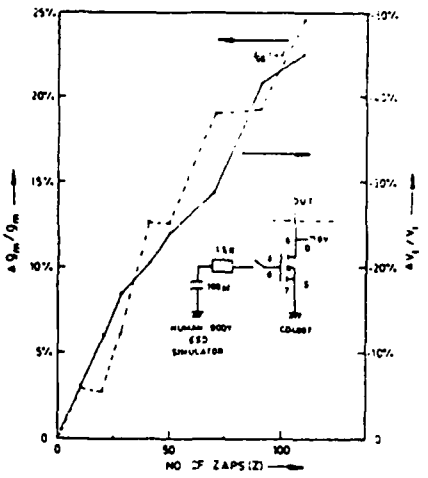


FIG.5 VARIATION OF g_m & V_t WITH RESPECT TO NUMBER OF ZAPS

NOISE PARAMETER & AGING MODEL

The fractional change in R_N as a function of the number of zaps can be calculated using Eqn. (3) and the measured data of Fig. 5. The corresponding results are presented in Fig. 6.

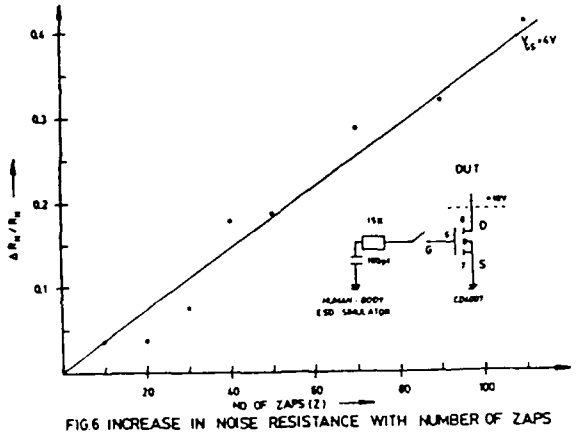


FIG.6 INCREASE IN NOISE RESISTANCE WITH NUMBER OF ZAPS

From the data presented in Fig. 6, it can be ascertained that $\Delta R_N/R_N$ is linearly proportional to Z (number of zaps), closely agreeing with the observations by Abovitz, et al [7]. Further, the rate of change of R_N is approximately twice as that of g_m. That is, the degradation can be more accurately assessed in terms of noise parameter measurements than by g_m determination.

Cumulative build-up of degradation with the recurrence of zaps amounts to a dormant stage of failure during which the device would exhibit a performance degradation leading to out-of-spec condition(s). This device-aging can be assessed by measuring the time variation of a nondestructive property (p) such as a noise parameter as indicated in the present analysis. Suppose two time-variation curves are obtained corresponding to two distinct (subcatastrophic) stress-levels. The functional form of p will be independent of the stress magnitude and the two curves will have the same shape, but different length (along the time axis) as shown in Fig. 7. The times corresponding to same (extent of) aging under two distinct stress levels can be denoted as t_1 and t_2 (Fig. 7) and are known as "equivalent times" [9]. By the application of "equivalent aging principle," it is possible to relate the equivalent times in terms of their corresponding stress levels, namely, V_1 and V_2. It is given by [9]

$$V_1^n t_1 = V_2^n t_2 = K_1 \text{ (Constant)} \tag{4}$$

where n is the endurance coefficient. Eqn. 4 can also be written in terms of the average numbers of zaps Z_1 and Z_2 occurred during the period t_1 and t_2, respectively. That is,

$$V_1^n Z_1 = V_2^n Z_2 = K_2 \text{ (Constant)} \tag{5}$$

Thus, from Eqn. 4 or 5, for a given severity level, the corresponding value of failure-time (or average number zaps during the period of failure-time) can be assessed by determining the values of n, K_1 and K_2.

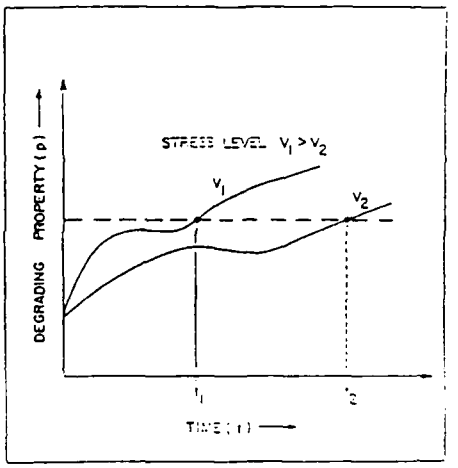


FIG.7 DEGRADATION VERSUS TIME UNDER TWO DISTINCT STRESS LEVELS

Further, the device reliability relevant to the endochronic degradation can be modeled by assuming that degradation rate is proportional to the existing degradation [10]. The proportionality constant is a positively distributed random variable and the extent of degradation would tend to be asymptotically log-normal. Hence the general form of life distribution Z (number of zaps) is given by

$$G(Z,p_c) = 1-\phi\left[\frac{\ln(p_c)-\mu}{\sigma}\right] \tag{6}$$

where ϕ is the standard normal distribution and $p_c = r - r_c$. Here $r = \Delta R_N/R_N$ and the suffix c depicts the critical value of r. Further ln (p_c) has a mean value of μ and a standard deviation of σ. This log-normal aspect of life-time statistics as applied to

endocronic degradation has been verified by the authors (with the MOS input leakage current as the control parameter, p) and the results are presented elsevhere [11].

CONCLUSIONS

From the results presented here, the following conclusions can be inferred:

1. Noise parameter changes in a MOS device subjected to electrical overstressings represent the global, time-dependent degradation.
2. Such noise parameter variation expressed in terms of the fractional change in the noise resistance (R_N), is explicitly related to two major MOS-device parameters, namely, g_m and V_t (Eqn. 3).
3. The rate of change of R_N with respect to the number of zaps is approximately linear.
4. Further, this rate of change of R_N is approximately twice the corresponding change in g_m.
5. Using $\Delta R_N/R_N$ as a control parameter (p), the principle of equivalent aging can be applied to MOS degradation for accelerated aging studies.
6. The degradation process can be modeled with log-normal distribution for relevant lifetime statistical analysis.

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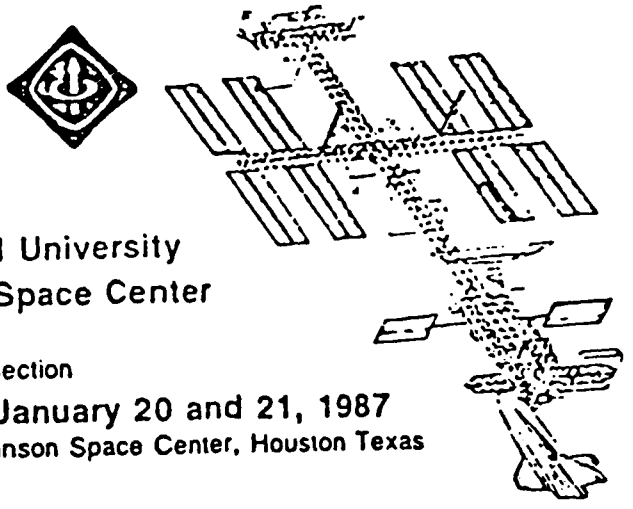
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INFLUENCE OF IONIZING RADIATIONS & ELECTRICAL OVERSTRESSINGS ON MOS DEVICES: A COMPARISON

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ANALOGOUS INFLUENCE OF IONIZING RADIATIONS AND ELECTRICAL OVERSTRESSINGS: DAMAGE CHARACTERIZATION VIA NOISE PARAMETERS

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Abstract

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INTRODUCTION

The knowledge of common mechanisms involved in the degradation process(es) due to external stimuli, such as ionizing radiations and electrical overstressings, is useful, not only in understanding the interactive physics involved, but also will enable a common hardening technique (process/design) to achieve protection against these stimuli. Such studies will further indicate a one-to-one correlation (in quantifiable terms) between the intensity/magnitude of an ionizing influence and an electrical overstress which may cause the same extent of damage. This equivalence will enable substitution of test method(s) to simulate failure/degradation effects. 'Oxide-charge and surface-effects' [1,2] observed under the influence of ionizing radiations or electrical overstresses result from positive charge build-up in the gate-oxide due to radiation-induced (or EOS-induced) creation of electron-hole pairs; and the trapping of holes at the silicon-to-oxide interface alters the device parameters, namely, the transconductance (g_m), MOS capacitance (C) and the threshold voltage (V_T). To understand the physics of these analogous effects observed, the mode(s) of energy transfer from the invasive external stimulus to the device interior, warrants unique modeling and analysis as discussed in this paper.

Inasmuch as all the degrading device parameters (g_m, C and V_T) are interdependent, the cohesive damage of the device would be assessed by an appropriate function which collectively represents the net physical damage due to external stimulus. It is presently demonstrated that noise characteristics can depict the global representation of stochastical variation [3] in charge-trapping and interface generation due to the external stimuli (ionizing radiations or EOS); relevant noise measurements of degraded devices can also be useful in accelerated test

procedures (using equivalent EOS to simulate ionizing radiations) adopted for life-time modeling strategies and in hardening effectiveness evaluation.

OXIDE-CHARGE & SURFACE EFFECTS

A MOS transistor can be looked at as a capacitor with the metal and semiconductor as the plates and the gate-oxide as the dielectric. Under ionizing radiation conditions, the ionization process is illustrated in Fig. 1. At $t^- = 0$ (Fig. 1a), the condition prior to irradiation is shown. At $t = 0$ (Fig. 1b), the ionizing energy is delivered to the oxide, and the electron-hole population is generated. Immediately after ionization, the process of electron-hole recombination will occur, but so will electron transport. But as electron mobility in the oxide at room temperature is approximately 20 cm^2/V-sec, and hole mobility is approximately $2 \times 10^{-5} cm^2$/V-sec, under the applied voltage, any electrons that do not undergo recombination will be swept to the gate and removed in picoseconds, leaving behind the less mobile holes. These holes will begin a transport process toward the silicon-to-oxide interface as shown in Fig. 1e. Some holes will pass into Si, while others will become trapped at defect centers very near the interface of the gate oxide and the bulk silicon.

Fig. 2 depicts the shift in the C-V curve associated with the entire process and the resulting permanent shift due to the trapped charge buildup. In the case of the N-channel device, the trapped positive charge will continue to build up and, in effect, make it easier to create the N-channel (inversion layer). This will lower the threshold voltage (Fig. 3). The reversal of threshold shift is caused by the saturation of surface traps and interface state generation at the silicon-to-oxide boundary occurring at higher levels of ionizing radiations. This mechanism of interface state generation is not well understood at this time except for a simple theory that two different crystal structures (silicon and oxide) meet to form an interface having some irregularities, the number of which increases with increased irradiation. In the case of a corresponding P-channel device, the buildup will make it more difficult to create an inversion layer (in an enhancement mode P-channel transistor). The effect of ionizing radiation on a P-channel threshold is shown in Fig. 3. The net effects of ionizing radiation on a MOS device as a function of threshold shifts are therefore: N-channel devices are easier to turn on or can actually become depletion mode; and P-channel devices become more difficult to turn on.

Similar oxide-charge and surface-effects also appear when a MOS structure is subjected to an EOS, say by a (positive) high-voltage at the gate. During the high-voltage pulses, electrons are injected into the gate-oxide via Fowler-Nordheim tunneling from the Si substrate, and some fraction of the injected electrons then create electron-hole pairs in the bulk of the oxide through impact ionization (Fig. 4a). The resulting electrons and holes behave similarly to those generated by ionizing radiation in MOS structures under positive (worst-case) bias (Fig. 4b): Most of the electrons are swept out of the oxide while the

holes drift under the positive field toward the oxide-to-silicon interface where they may be removed or trapped. Some of these holes may also cause interface states to be produced. The resulting flatband-voltage shift and interface-state build-up can be depicted as in Fig. 2.

Ionizing radiations or electrical overstressings will also cause carrier mobility degradation because of the presence of trapped charges near the silicon-to-oxide interface and interface generation, of which interface generation is more dominant and it becomes negligible at lower levels of ionizing radiations/EOS. As the stressing levels are increased (about a million rad for ionizing radiations or 9MV/cm for EOS), mobility degradation will affect P and N-channel device performance, with increased interface states being the primary cause of degradation. This mobility degradation can be observed via transconductance (g_m) measurements. Another performance problem induced by ionizing radiations or EOS is the increase in leakage current due to surface effects.

MOSFETs stressed by ionizing radiations or by EOS have the tendency to anneal. Annealing is the time-dependent detrapping of trapped charge at the silicon-to-oxide interface. It is sometimes referred to as a self-healing effect. However, the time constant involved is in the order of minutes to over one year, depending on the extent of damage, design-based on-chip protection and the type of processing. Though the surface states generated are relatively permanent, it can also be annealed with high temperatures (>125° C). Any lattice damage (interstitials, vacancies), however, is irreversible.

Experimental studies indicate that trapping of holes or oxide-silicon interface degeneration does not differ significantly between electrical overstressing and ionizing irradiations [4] despite the fact that holes are transported to the interface rather under high field conditions in EOS phenomenon; whereas, hole transport under ionizing irradiations is not field activated. Hence, it is evident that capture of hole by a trap at the interface is not a strong function of electric field in the oxide.

SINGLE-MODEL REPRESENTATION OF IONIZING RADIATION AND EOS EFFECTS

On the basis of aforesaid discussions, the identical effects observed in MOSFETs when subjected to ionizing radiations or EOS can be summarized as follows: 1) Shift in threshold voltage; 2) Change in oxide-capacitance; 3) Mobility (μ) degradation; 4) Change in transconductance; 5) Increase in leakage current; and 6) Annealing. These various parameters though can represent the degradation (either due to ionizing radiations or due to EOS) independently are, however, interdependent and explicitly related through analytical expressions. Therefore, it is possible to establish a general expression which uniquely represents the cohesive damage, irrespective of the nature of external stimulus. For this purpose the global effect of stochastical variations in charge-trapping and interface generation (under external stimulus) can be considered to model the net physical degradations observed. And as these stochastical fluctuations in the device-interior

manifest as the 'device-noise,' the desired modeling can be characterized by appropriate noise parameters of the device.

When a MOS device is subjected to external stress (either ionizing radiations or EOS), the corresponding induction of charge-trapping and generation of interface states can be equivalently represented by an input noise resistance R_N given by [5]

$$R_N \simeq C_o N_s (\mu_s/\mu_o)^2 \tag{1}$$

where C_o is a constant, N_S is the surface-state density and μ_s/μ_o refers to the field-effect mobility to low-field mobility ratio. Eqn. (1) indicates that R_N is directly proportional to N_S concurring with the experimental results due to Abowitz, et al [6]. Hence the time-dependent history of N_S as controlled by any external overstressings can be tracked via the assessment of R_N. Further, the field-effect mobility is also dependent on N_S and is therefore linked with g_m and V_T of the device. Explicitly,

$$\frac{\mu_s}{\mu_o} \simeq \frac{1}{1+\alpha N_S} \simeq \frac{g_m}{g_{mo}} \simeq \frac{1}{1+\beta(V_G-V_T)} \tag{2}$$

Here, α and β are constants and g_{mo} refers to the value of g_m under unstressed conditions and V_G denotes the applied gate potential.

From Eqns. (1) and (2), the following relation can be obtained:

$$\frac{\Delta R_N}{R_N} \simeq \frac{\Delta g_m}{g_m}\left[2 - \frac{1}{1-\frac{\Delta V_T}{V_T}\,\frac{1}{(V_G-V_T)\beta}}\right] \tag{3}$$

The constant β has the approximate values of 0.138 and 0.308 for the N-channel and P-channel MOSFETs, respectively [4]. More generally, V_G can be expressed in terms of the electric field across the gate-oxide, namely, E_G. That is, $V_G = E_G t_{ox}$, where t_{ox} is the gate-oxide thickness. While E_G refers to the electric field intensity corresponding to an electrical overstress (EOS) phenomenon, it is possible to establish an equivalent E_G to represent the ionizing radiation dosage, which produces the same extent of degradation expressed via noise parameter of eqn. (3). Let D_I be the dosage delivered (or, absorbed dosage) to an oxide-gate, which through ionization process creates a hole density (area density) of Q_R equal to $K_I t_{ox} D_I F(E_G)$ where K_I is the infinite field ionization coefficient [4]

equal to 1.22×10^{-6} C $CM^{-3}rad^{-1}$ (SiO_2) and $F(E_G)$ is the E-field dependent charge-yield parameter [4] with approximate value of 0.83 at E_G = 1MV/cm. If the same hole-density of Q_R has to be stimulated by an electrical overstress phenomenon (via high field injection of electron current density through Fowler-Nordheim tunneling by the gate-oxide field-intensity, E_G), the corresponding current density (j) can be expressed (by neglecting space-charge effects) as equal to $AE_G^2 \exp(-B/E_G)$ where A and B are constants. The best estimates of [4] A and B are 2×10^6 amperes/$(MV)^2$ and 238 MV/cm, respectively. Therefore EOS-equivalent of Q_R can be written as

$$Q_R \text{ (EOS)} = j\alpha\, t_{ox}\, \Delta t \tag{4}$$

where α is the probability per unit length that an injected electron will create an electron-hole pair and is equal to $\alpha_o \exp(-H/E_G)$ where $\alpha_o \simeq 6.5 \times 10^{11}$ cm^{-1} and H~ 180MV/cm [4].

Further, Δt in eqn. (4) specifies the duration of EOS event. Assuming that lightning function of the form $e_1(t) = E_G [\exp(-Ct)-\exp(-Dt)]$ to represent the transient electrical overstressing, the duration, Δt is given by

$$\Delta t = [(D-C)/CD] [\exp(-Ct_m)-\exp(-Dt_m)]^{-1} \tag{5}$$

where t_m is the rise-time of the transient equal to $\ln(D/C)/(D-C)$. The values of C and D can be explicitly specified for a given type of EOS event, such as human-body ESD model, etc., and are dependent on the peak value of the stressing potential, V_G.

Combining eqn. (4) and eqn. (5), the equivalent dosage D_I can be expressed as

$$D_I = \alpha_o A E_G^2 [(D-C)/CD] [\exp(-Ct_m)-\exp(-Dt_m)]^{-1} \exp[-(H+B)/E_G] \tag{6}$$

Hence, using approximate values for the parameters discussed previously, the expression for D_I reduces to

$$D_I \simeq 10^{24} (V_G/t_{ox})^2 \exp(-418\, t_{ox}/V_G) \Delta t(V_G) \tag{7}$$

where V_G is expressed in MV, t_{ox} in cm and Δt is functionally dependent on V_G.

Considering a typical electrical overstressing due to an electrostatic discharge (ESD) of subcatastrophic level (say V_G = 50V peak) from a finger tip (Fig. 5) across a gate-oxide of thickness 30 *nm* over a pulse-duration, Δt = 10n sec, the corresponding equivalent radiation dosage is approximately equal to 36 M rad (SiO_2). That is, this ESD event would introduce as many holes into the oxide as a 36 M rad (SiO_2) of ionizing radiation.

RELATIVE NOISE PERFORMANCE UNDER EOS AND IONIZING IRRADIATIONS

For a given injected electron fluence ($Q_I = j\Delta t$), the relative damage introduced in the MOSFET by an EOS and an ionizing radiation can be estimated as follows: By virtue of one-to-one equivalence between the magnitude of EOS and ionizing dosage, the relative damage expressed, say, in terms of threshold shift $\Delta V_T/V_T$ can be written as a linear proportionality relation of the form $\Delta V_T(EOS)/V_T = K\ \Delta V_T(RAD)/V_T$ where K is a constant.

Considering the results due to Boesch and McGarrity [4], for a given amount of injected electron fluence ($1.9 \times 10^{-5} C/cm^2$), the theoretical and experimental results corresponding to high field stressing of 9MV/cm) and ^{60}Co irradiation (10^4 rad SiO_2) on a t_{ox} = 1000 Å MOS structure, the value of K is found to be approximately equal to 2.3; or, in general, K>1. Hence, using the linear relation between $\Delta V_T(EOS)/V_T$ and $\Delta V_T(RAD)/V_T$, it can be shown that $\Delta R_N(EOS)/R_N$ is nearly equal to $(4/3)\Delta R_N(RAD)/R_N$. In other words the damage, manifesting as the device noise under EOS injecting a given amount of electron fluence into the gate, is approximately 25% more, for the same extent of electron fluence injected by a radiation source. Typical noise parameter ($\rho = \dfrac{\Delta R_N/R_N}{\Delta g_m/g_m}$) variations as functions of radiation dosage for a P and N channel MOSFETs are shown in Figs. 6 and 7. Corresponding variations of threshold voltage, V_T are also depicted in Figs. 6 and 7, from which it can be observed that the noise parameter follows the trend of V_T variations(s).

Will radiation hardening concurrently improve static-protection or vice versa? The observed similarities suggest the possibility of formulating a one-to-one equivalence of modeling of radiation damage versus EOS effects from which it can be extrapolated that any scheme that is implemented (either via processing or via design methods) to prevent/reduce radiation-induced (deleterious) effects may also subdue the influences of EOS effects. In other words radiation hardening schemes (process/design) with a few optimization changes may provide dual protection to prevent/reduce gate-oxide damages arising from ionizing radiations or from EOS. In order to achieve effective dual protection through optimization of process/design techniques, basic

research is required to determine this ionization radiation-to-EOS equivalence so that the common-to-both type of damages(s) in the gate-oxide can be effectively prevented through optimization procedures.

CONCLUSIONS

This work provides a basic insight into the problem of a comparative study relating ionizing radiations and EOS effects on MOS devices. The results indicate a strong correlation between the two effects cited, which suggests the feasibility of designing common countermeasures, as well as adopting substitutions in the analysis and/or simulation techniques.

ACKNOWLEDGEMENT

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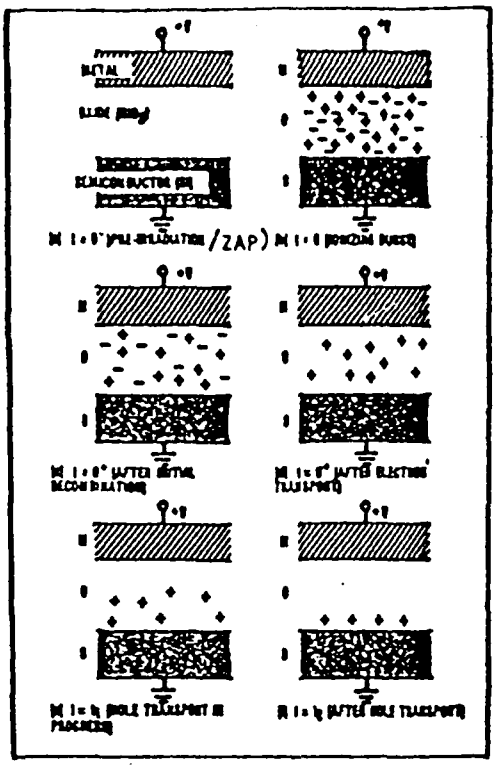


FIG. 1 CARRIER TRANSPORT MECHANISM

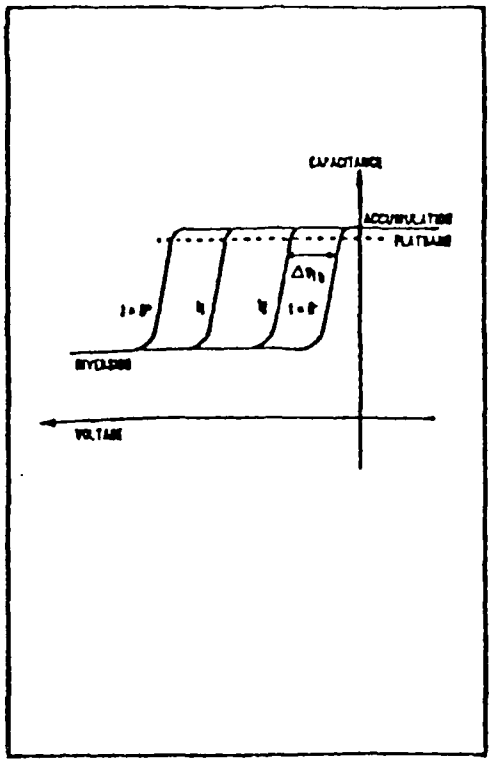


FIG. 2 C-V CURVES FOR CONDITIONS IN FIG. 1

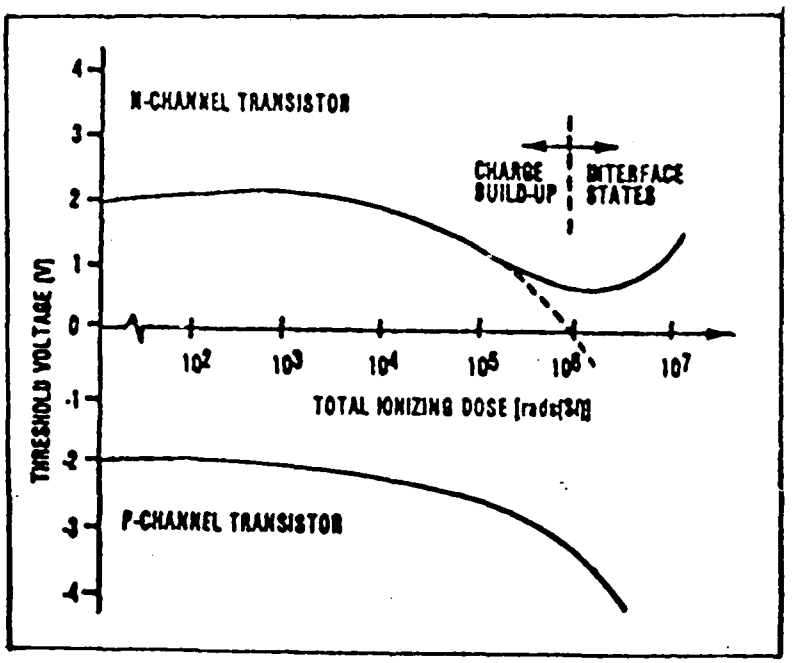


FIG. 3 RADIATION EFFECTS ON P AND N CHANNEL MOSFETS.

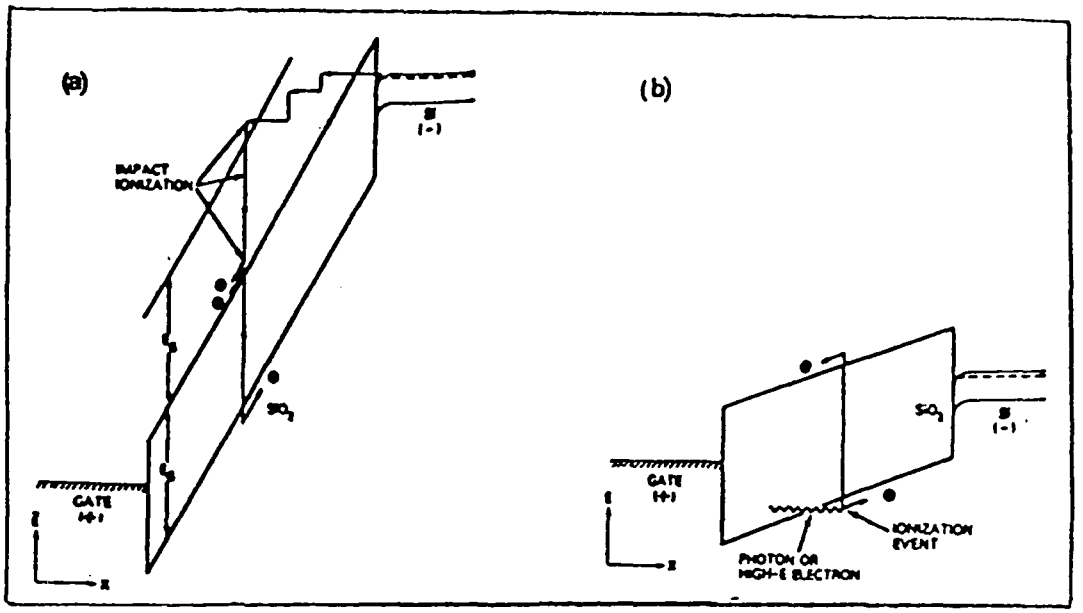


FIG. 4 CREATION OF ELECTRON - HOLE PAIRS DUE TO: (A) HIGH-FIELD INJECTION AND (B) IONIZING RADIATION

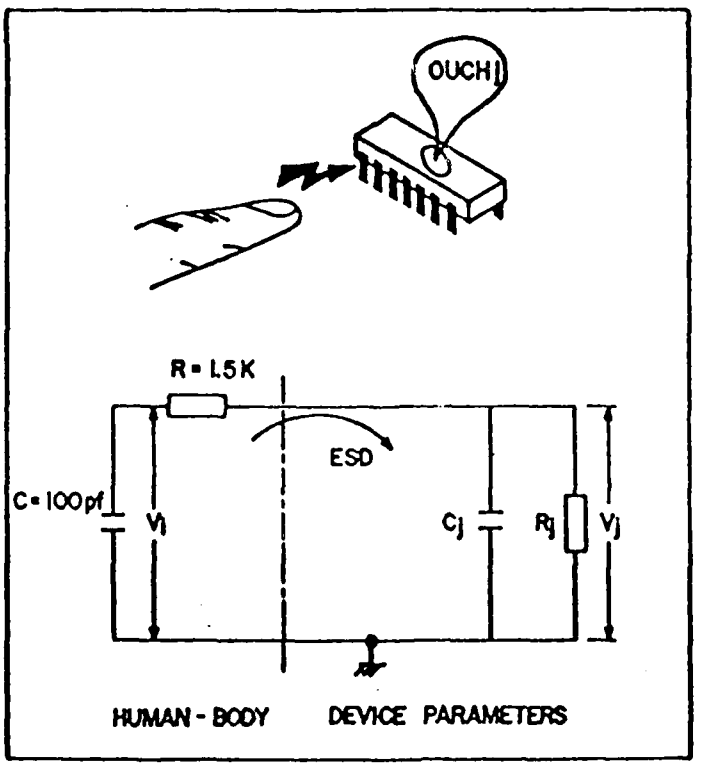


FIG. 5 ESD: HUMAN-BODY MODEL

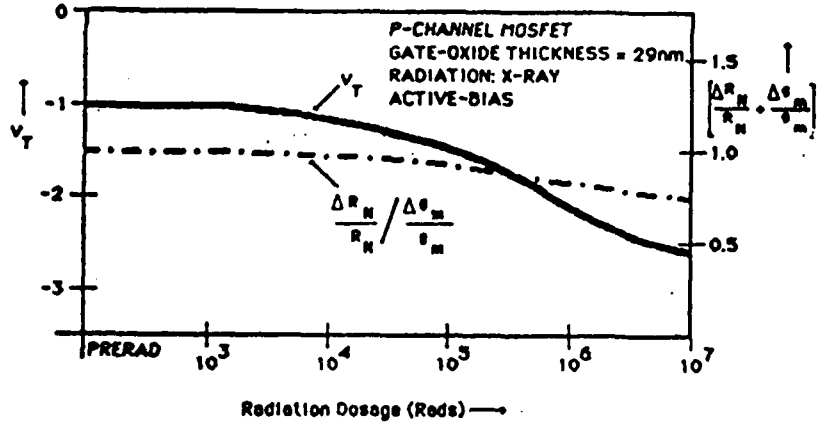


FIG.6 RADIATION DOSAGE VERSUS THRESHOLD VOLTAGE (V_T) AND NOISE PARAMETER ($\Delta R_N / R_N + \Delta g_m / g_m$)

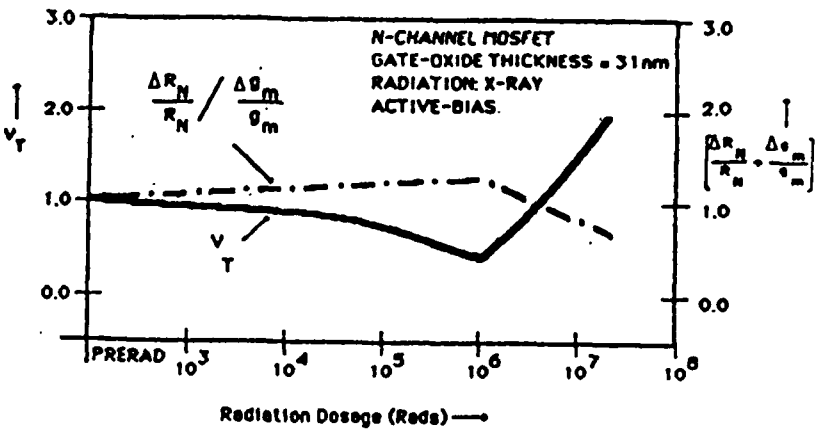


FIG.7 RADIATION DOSAGE VERSUS THRESHOLD VOLTAGE (V_T) AND NOISE PARAMETER ($\Delta R_N / R_N + \Delta g_m / g_m$)

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NOTE

NOISE CHARACTERISTICS OF IONIZING-RADIATION STRESSED MOSFET DEVICES

INTRODUCTION

It has been known for years that ionizing radiations can change the electrical properties of solid state devices, leading to possible system failure [1]. In particular, gamma rays, X-rays and neutron bombardment have proven most harmful. Among the LSI devices, MOS circuits are highly sensitive to damages under critical radiation environments. The primary failure mode and/or degradation of MOSFETs resulting from ionizing radiations is due to the 'oxide-charge and surface-effects,' [2], occurring in the gate-oxide and/or field-oxide regions. The effects of ionizing radiations are mainly threshold voltage shift and channel mobility degradation caused by the creation of electron-hole pairs and trapping of holes at the $Si-SiO_2$ interface [2]. The net effect of charge-trapping and the associated occupation of surface states can also be viewed as a random/stochastical phenomenon which can be characterized by a global noise parameter. Such a representation/model will be useful to study the noise performance of the device under radiation environments as indicated in the present work.

NOISE-MODEL

The global effect of 'oxide-charge and surface-effects' described above can manifest as the device noise which can be quantitatively represented by a noise-model as described below:

Following the analysis by Leventhal [3], the effect of charge-trap induction and generation of interface states can be equivalently represented by an input noise resistance R_N given by

$$R_N = C \left(\frac{\mu_S}{\mu_o}\right)^2 N_S \qquad (1)$$

where C is a constant of proportionality and N_S is the surface-state density; μ_s/μ_o refers to the field-effect mobility to low field-effect mobility ratio. Further, inasmuch as field-effect mobility is also dependent on N_S and is, therefore, linked with the device transconductance (g_m) and the threshold voltage (V_T) [4,5], the following relation can be obtained [6] from eqn. 1. (Note the typographical errors in [6]: eqns. 1 and 3 of [6] should read as *eqns.* 1 and 2 of the present paper, respectively.)

$$\frac{\Delta R_N}{R_N} = \frac{\Delta g_m}{g_m} \left[2 - \frac{1}{1 - \frac{\Delta V_T}{V_T} \cdot \frac{1}{(V_G - V_T)\beta}}\right] \qquad (2)$$

where ΔV_T is the threshold-voltage shift and β is a constant, approximately equal to 0.138 and 0.308 for the N-channel and P-channel MOSFETs, respectively [5].

The quantity V_G in eqn. 2 represents an 'equivalent gate-potential' which would inject the same electron-fluence into the gate equal to that injected by the ionization irradiation. V_G can also be expressed in terms

of an 'equivalent electric field' across the gate-oxide, namely E_G. That is, $V_G = E_G\ t_{ox}$, where t_{ox} is the gate-oxide thickness.

This equivalent electric stress parameter E_G, can be specified explicitly in terms of the radiation dosage, D, assuming that, over a duration of Δt, the effect of E_G or D is to inject the same extent of electron fluence, namely $j\Delta t$, where j is the current density. Hence, relevant analysis yields,

$$D \simeq A\ E_G^2\ \Delta t\ \exp\ (-B/E_G) \qquad (3)$$

where A and B are constants approximately equal to 10^{24} and 418, respectively [7], if E_G is expressed in MV/cm. Thus for a given dosage level of D, using eqns. 2 and 3, the noise performance of the device can be decided quantitatively.

TEST STUDIES & CONCLUSIONS

Variations of the noise parameter $\frac{\Delta R_N}{R_N} / \frac{\Delta g_m}{g_m}$ corresponding to a P-channel and an N-channel MOSFETs as functions of the radiation dosage (X-ray), are depicted in Figs. 1 and 2. Also shown in Figs. 1 and 2 are the threshold voltage shifts in the P- and N-channel MOSFETs [8]. The results on noise parameter presented in Figs. 1 and 2 are calculated via eqns. 2 and 3, using the available data on threshold voltage shifts versus radiation dosage [8]. From the results shown, the following can be inferred:

1. Damage introduced by ionizing radiations in a semiconductor device (such as MOSFET) can also be characterized by the noise performance of the device.

2. The noise parameter, as a function of radiation dosage tends to track closely the variation of V with respect to the dosage level. This is true for both P- and N-channel MOSFETs (Figs. 1 & 2). The percentage shift in the magnitude of noise parameter, for a given level of radiation dosage is, however, less than the corresponding percentage shift in the threshold voltage. Referring to Fig. 1 , (P-MOS) for a dosage level of 10^7 rad (Si), V_T shifts by 170%, whereas the noise parameter changes only by 26%. Similarly in Fig. 2 (N-MOS), V_T shifts for 10^6 and 10^7 rad (Si) are -52% and +42%, respectively. However, the corresponding noise parameter shifts are +28% and -8%, respectively. Thus, for a given level of irradiation, the variation in V_T is more overwhelming than changes in noise performance.

3. Nevertheless, in low noise applications of the device, the influence of ionizing radiations should be duly accounted for in the system design as noise performance degradation is inevitable as a result of radiation-induced oxide effects. While 'single event' upsets due to ionizing radiation usually cause concern in digital circuits, noise performance degradation due to cumulative/total ionizing irradiations may require specific attention in linear devices. Especially, as the device is stressed repeatedly, the device damage (noise performance degradation) will cumulatively increase. Such endochronic degradation response would be detrimental for low-noise system operation. The present analysis is useful in the relevant studies.

4. The simple model presented here provides a quantitative approach to determine the noise performance of a MOSFET ionizing irradiations. The relevant calculations are useful to determine the extent of radiation hardening required to achieve a given level of low noise performance of the device under ionizing radiation environments. And, noise monitoring can serve as an adjunct support to conventional V_T and C_{ox} estimations adopted in hardness assurance efforts.

5. The present work models only the effect(s) of ionizing radiations on the device-noise. Should the geometrical parameters (such as the channel length) change, the transconductance would be significantly affected (especially in short-channel devices) and the relevant noise-model will be more involved. Related studies are in progress.

6. It can be shown that $\Delta g_m/g_m \simeq \Delta V_T/(V_G-V_T)$. Hence, the noise-parameter profiles of Figs. 1 and 2 will remain the same (except for a scale-factor) if the noise-parameter is normalized with respect to threshold-voltage shift.

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CAPTIONS FOR THE DIAGRAMS

Fig. 1 Threshold voltage and noise parameter versus total radiation dosage (P-Channel MOSFET).

Fig. 2 Threshold voltage and noise parameter versus total radiation dosage (N-Channel MOSFET).

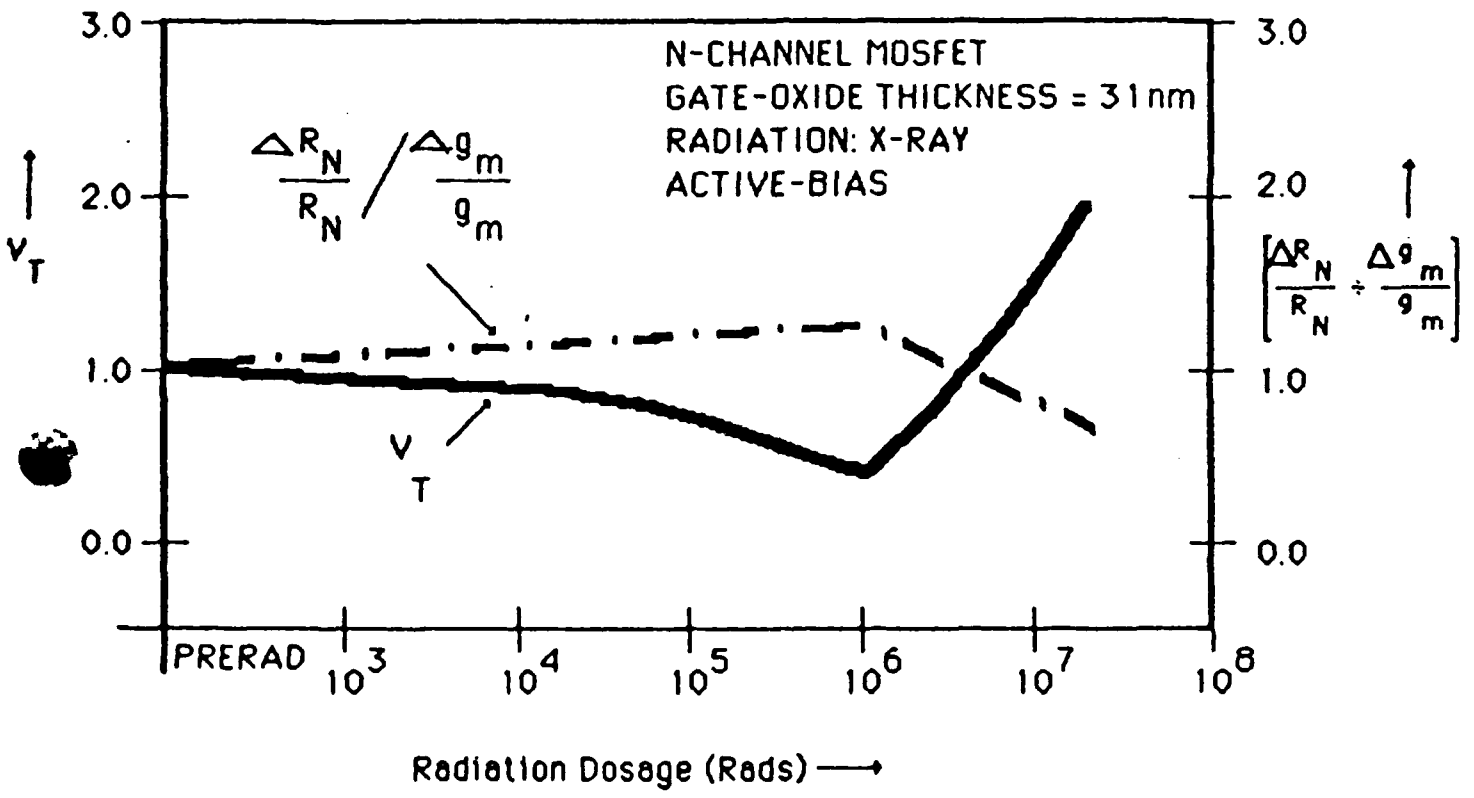


FIG. 2 THRESHOLD VOLTAGE (V_T) AND NOISE PARAMETER ($\Delta R_N / R_N \div \Delta g_m / g_m$) VERSUS RADIATION DOSAGE

N-CHANNEL MOSFET

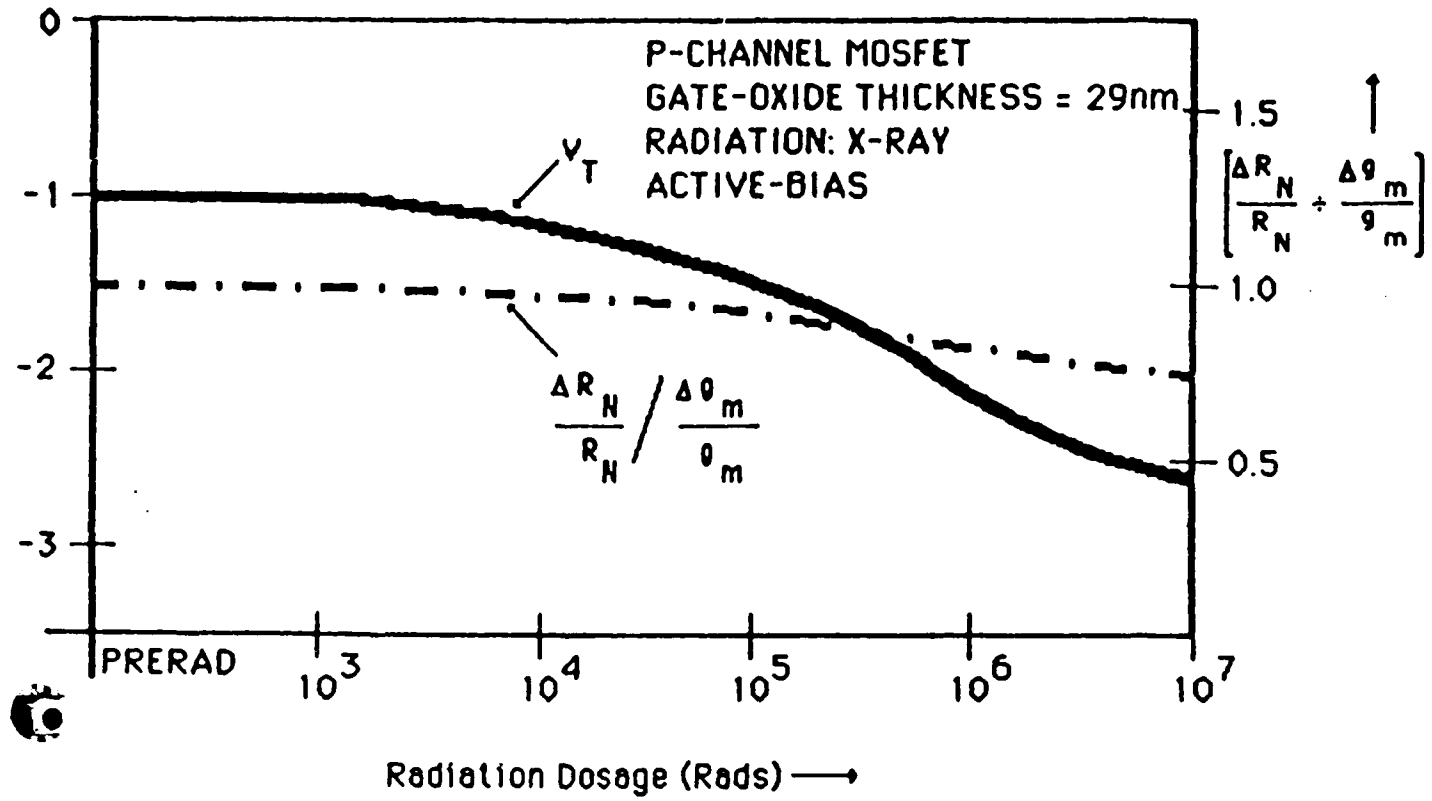


FIG. 1 THRESHOLD VOLTAGE (V_T) AND NOISE PARAMETER ($\Delta R_N / R_N \div \Delta g_m / g_m$)

VERSUS RADIATION DOSAGE

P-CHANNEL MOSFET

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Electrostatic Discharge (ESD), Electrical Overstressing (EOS), Thin-Oxide Dielectric Breakdown

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Non-explicit severity of overstressings due to geometrical and material characteristics and/or perturbations at the gate-oxide region in a MOS structure is studied.

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BREAKDOWN IN AN ELECTRICALLY OVERSTRESSED THIN-OXIDE OF A MOS CAPACITOR: NONEXPLICIT SEVERITY DUE TO GEOMETRICAL PERTURBATIONS

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ABSTRACT

Scaling-down efforts and process variations will cause involuntary perturbations in the geometry of gate-oxide region of a MOS structure. Such stochastical variations will significantly influence the breakdown mechanism at the thin gate-dielectric. Expressions to depict the enhanced severity of overstressings due to such perturbations are derived. Competing influence of scaling-down and the perturbations is elucidated.

INTRODUCTION

Submicron implementation with acceptable reliability warrants a thorough understanding of the physics of thin-oxide breakdown in MOS structures under electrical overstressings so as to seek preventive solutions against high-

stress failures [1]. Existing studies address the direct influence of oxide-thickness, crystal purity/contamination, dielectric integrity, processing methods [2] and the characteristics of overstressing voltages on the breakdown mechanism [3,4,5]. And simulation studies are done on tailor-made MOS structures with Al, Mo, Wo, polysilicon or silicide field-plate(s) of circular or rectangular geometry, the substrate being p- or n-type material [6,7].

In these studies, however, effects of field-plate dimensions and stochastical variations/perturbations in the geometry of the gate-oxide region [8] have not been seriously considered in depicting the breakdown model of MOS capacitors; only, some experimental results from post-breakdown examinations have been compiled [3] which indicate the clustering of failure sites being about 80% at the corners of rectangular/square field-plate(s). Qualitative explanation based on electric field fringing at the corners have been presented to justify the observed data.

Invariably, changes in the design (geometrical scaling-down), processing methods and optimized material selection decide the field-plate and gate-oxide dimensions as well as the geometrical perturbations [8,9,10] involved; and in order to determine the corresponding electrical overstressing (EOS) threat on a priori basis, an exclusive analysis formalizing the extent to which breakdown will be influenced by the geometrical parameters (perturbed and/or unperturbed) is imminent. Studies presented here will determine this overextending severity.

THEORETICAL FORMULATION

Unperturbed MOS structure: Fig. 1 depicts a MOS capacitor with a rectangular field-plate of unperturbed boundary and separated by a thin oxide-dielectric from a semi-infinite substrate. Should the breakdown due to an applied voltage ϕ_G occur, the potential distribution (ϕ) below the field-plate can be determined by solving the differential equation with appropriate boundary conditions. Thus, referring to Fig. 1, the injected current (I) upon breakdown is assumed to be evenly distributed over the length (L) of the plate and flows in the y-direction down the field-plate from the runner metallization over the width W. With a dimensionless constant Y = y/W, the differential equation governing the potential distribution (ϕ) in the post-breakdown dielectric gate-region can be written as

$$d^2\phi/d^2Y^2 = 2k_1\phi \tag{1}$$

where $k_1 = \sigma_{ox}W^2/(t_{ox}t_f\sigma_f)$. Here σ_{ox} and t_{ox} depict the post-breakdown oxide conductivity and the gate-oxide thickness, respectively. Likewise σ_f and t_f represent the electrical conductivity and the thickness of the field-plate, respectively. Equation (1) can be solved with the boundary conditions, namely, $\phi = \phi_G$ at Y = 0 and $d\phi/dy = 0$ at Y = 1. The result is

$$\phi = A \exp(\sqrt{2k_1}Y) + B \exp(-\sqrt{2k_1}Y) \tag{2}$$

where

$$A = \phi_G/\{\exp\ [2\sqrt{2k}_1]-1\} \text{ and}$$

$$B = \phi_G\ \exp\ [2\sqrt{2k}_1]/\{\exp\ [2\sqrt{2k}_1]-1\}.$$

From the expression of equation (2) derived for the post-breakdown potential distribution (ϕ) under the field-plate, it is possible to quantify the extent to which the electrical conductivity and finite thickness of the field plate would influence or distort the uniform current flow vertically beneath the field-plate. Inasmuch as the gate-oxide breakdown is significantly affected by this nonuniform potential/current distribution, a quantifiable measure of this nonuniformity would specify the severity of overstressing. Assessment of this severity parameter will enable distinguishability between the breakdown due to loss of dielectric integrity and that caused by field-plate induced nonuniform electric-flux concentrations. That is, the severity of electrical overstressing due to uneven current/potential distribution caused by the finite thickness and conductivity of the field plate can be expressed by a Severity Factor (SF) denoting the ratio of maximum current density to the uniform current density. For the unperturbed rectangular geometry of Fig. (1), it can be shown that,

$$SF_U = \sqrt{2k}_1/\tanh\sqrt{2k}_1 \qquad (3)$$

where the suffix U depicts the unperturbed status.

In practical devices, using thin field-plates of Al, W, Mo, polisilicon, silicide, or polycide (like $MoSi_2$) materials, the magnitude of k_1 is very large and therefore the severity expression of (3) reduces to (via large argument approximation):

$$SF_U \simeq \sqrt{2}k_1 \quad >>1. \tag{4}$$

MOS structure with perturbed rectangular boundary: Fig. 2 depicts a MOS structure with a gate-oxide region having a stochastic edge. The randomness of the rectangular boundary is specified by a stochastical variable Δr, so that any point r on the rectangle corresponds to a point $r + \Delta r$ on the real/perturbed boundary as indicated in Fig. 3, where $\overline{u}_n$ and $\overline{u}_t$, respectively, denote the normal and tangential unit vectors. For simplicity Δr is presumed to be directed along $\overline{u}_n$.

The post-breakdown potential ϕ, in the oxide region can be implicitly expressed by means of an auxiliary potential ψ given by

$$\psi = \int_{\phi_S}^{\phi_G} \sigma_{ox}(\phi)d\phi \tag{5}$$

where ϕ_s is the post-breakdown voltage-drop across the substrate region. The function ψ satisfies Laplace's equation, namely $\nabla^2\psi = 0$ with the boundary conditions $\psi = \psi_s$ at $x = 0$ and $\nabla\psi.\bar{u}_n=0$ all along the rectangular boundary.

With the specified perturbations, spatial distribution of ψ can be written in terms of the zeroth and first order approximations as

$$\psi(r) = \psi_o(\bar{r}) + \psi_1(\bar{r}) \qquad (6)$$

and the corresponding boundary conditions can be approximately specified as $\psi_o(\bar{r}) = \psi_s$ and $\psi_1(\bar{r}) \simeq 0$ at $x = 0$. Also, $\nabla\psi_o.\bar{u}_n = 0$ and $\nabla\psi_1.\bar{u}_n = -\Delta r\,\partial^2\psi_o/\partial n^2 + \partial/\partial r(\Delta r)\ \partial/\partial t\ (d\psi_o/dt)$ along the perturbed boundary. Here n and t, respectively, denote the normal and tangential coordinates at any given point on the boundary. Further ψ_o and ψ_1 should independently satisfy the Laplace's relation, namely, $\nabla^2\psi_o = 0$ and $\nabla^2\psi_1 = 0$.

The zeroth order current density (J_o) in the oxide-region under post-breakdown condition can be written as equal to $(\sigma_{ox}/t_{ox})\ (\psi_G-\psi_s)$; and the corresponding first-order current density (J_1) can be derived from the auxiliary potential ψ_1 specified in terms of the Green's function $G(r/r')$, satisfying the two-dimensional differential equation $\nabla^2G(\bar{r}/\bar{r}') = \delta(\bar{r}-\bar{r}')$ with appropriate

boundary conditions [11]. (Here, δ represents the delta-dirac function.) In general, via Green's theorem,

$$\psi_1(r') = \oint [G(\bar{r}/\bar{r}')\nabla\psi_1(\bar{r}).\bar{u}_n - \psi_1(\bar{r})\nabla G(\bar{r}/\bar{r}').\bar{u}_n]dt. \tag{7}$$

With necessary simplifications, the following approximate solution for J_1 can be derived from ψ_1 of (7)

$$J_1 = -(\sigma_{ox}/t_{ox}\sqrt{LW})\ (\psi_G-\psi_s) \oint \Delta r dt \tag{8}$$

the integration being along the boundary. The negative sign in (8) depicts the decrease in the current density for any deviations in the original geometry. Further, the perturbed boundary of Fig. 2, has an expectation value $\langle\Delta r\rangle$ equal to zero so that the mean value $\langle J_1\rangle$ also vanishes. The variance of J_1 can be calculated from (8) as follows:

$$\sigma_J^2 = \langle J_1^2\rangle = (\sigma_{ox}/t_{ox}LW)^2(\psi_G-\psi_s)^2 \oint dt_1 \oint \langle\Delta r(\bar{r}_1)\Delta r(\bar{r}_2)\rangle dt_2 \tag{9}$$

where $\langle\Delta\bar{r}(r_1)\Delta r(\bar{r}_2)\rangle$ is the autocorrelation function [12]. For large correlation distance α of the perturbations (comparable to the device dimensions), the autocorrelation function is given by

$$\langle \Delta r(\bar{r}_1)\Delta r(\bar{r}_2)\rangle = \sigma_o^2 \exp\left[(-\Delta t)^2/2\alpha^2\right] \tag{10}$$

where σ_o is a constant and Δt is the tangentially measured distance between the points at $\bar{r}_1$ and $\bar{r}_2$. However, for a small correlation distance, the autocorrelation function can be simplified to $\sigma_o^2\sqrt{2\pi}\alpha\delta(\bar{r}_1-\bar{r}_2)$ and the corresponding variance of J_1 is given by

$$\sigma_J^2 = (\sigma_{ox}/t_{ox}LW)^2(\psi_G-\psi_s)^2\sqrt{2\pi}\ \sigma_o^2\ \alpha \oint dt_1 \quad . \tag{11}$$

Here $\oint dt_1$ is the rectangular periphery equal to 2(L+W). Hence, with respect to the zeroth order current density J_o, the relative rms deviation is given by

$$R_1 = \sqrt{\langle J_1^2\rangle}/J_o = \sigma_o\ \sqrt{\sqrt{8\pi}\ \alpha\ (L+W)}/LW. \tag{12}$$

And the corresponding severity factor is equal to

$$SF_{Pl} = \sqrt{2k}_1\ (1+R_1). \tag{13}$$

(Suffix P here denotes the perturbed status.)

MOS structure with perturbed oxide-thickness and of unperturbed rectangular gate-oxide boundary: Relevant configuration is illustrated in Fig. 4, where the mean oxide-thickness t_{ox} has a variation denoted by a two-dimensional stochastical process d(x,z). The corresponding post-breakdown conductivity of the oxide-region is decided by the perturbed local electrical field and hence by the potential ϕ. That is,

$$\sigma_{ox} \simeq f_1(\phi) + df_2(\phi) \tag{14}$$

where f_1 and f_2 are known functions of ϕ. Hence, using the condition $\nabla(\sigma_{ox}\nabla\phi) = 0$, under small perturbation approximation, the potential ϕ can be expressed as a correction of its zeroth-order value, ϕ_o as follows:

$$\nabla[f_1(\phi)\nabla\phi] = -\nabla.[df_2(\phi_o)\nabla\phi_o]. \tag{15}$$

Defining an auxiliary potential, $\nabla\psi = f_1(\phi)\nabla\phi$ (or, $\psi = \int_{\phi_S}^{\phi_G} f_1(\phi)\, d\phi$), it follows that

$$\nabla^2\psi = -\nabla.[df_2(\phi_o)\nabla\phi_o] \tag{16a}$$

and

$$\nabla\psi_o = f_1(\phi_o)\nabla(\phi_o). \tag{16b}$$

Further, application of Green's theorem to (16) leads to,

$$\psi(\bar{r}') = \psi_o(\bar{r}) + \int_S\int d(\bar{r}) f_2(\phi_o)\nabla\phi_o . \nabla G(\bar{r}/\bar{r}')dS \tag{17}$$

with the surface integration performed over the area S enclosed by the rectangular boundary.

The corresponding first-order term of the post-breakdown current density, J_1 can be expressed as

$$J_1 \simeq (\sigma_{ox}/t_{ox}LW)[t_{ox}/(\psi_G-\psi_s)] \int_S\int [d(\bar{r}) f_2(\phi_o)\nabla\phi_o . \nabla\psi_o]dS \tag{18}$$

the variance of which is given by

$$\sigma_J^2 = \langle J_1^2\rangle = (\sigma_{ox}/t_{ox}LW)^2(t_{ox}/\psi_G-\psi_s)^2 \int_S\int dS_1 \int_S\int \langle d(r_1)d(r_2)\rangle \times$$

$$[f_1(\phi_o)\nabla\phi_o . \nabla\psi_o]_1 [f_2(\phi_o)\nabla\phi_o . \nabla\psi_o]_2 dS_2 \tag{19}$$

where $\langle d(\bar{r}_1)d(\bar{r}_2)\rangle$ is the autocorrelation function of the oxide-thickness variations, d. For small perturbations (in comparison with the device

dimensions), $\langle d(r_1)d(r_2)\rangle \approx \sigma_o^2 2\pi\beta^2\delta(r_1-r_2)$ where β is the correlation distance; therefore,

$$\sigma_J^2 = [\sigma_{ox}/t_{ox}LW)^2[\sigma_o{}^2\ 2\pi\beta^2 t_{ox}^2/(\psi_G-\psi_S)^2] \int_S \int f_2^2\ (\phi_o)(\nabla\phi_o \cdot \nabla\psi_o)^2 dS$$

$$\approx (\sigma_{ox}/t_{ox}LW)^2[\sigma_o^2 2\pi\beta^2(\psi_G-\psi_S)^2/t_{ox}{}^2] \int_S \int f_2^2\ (\phi_1)\ dS \quad . \tag{20}$$

The ratio $f_2(\phi_o)/f_1(\phi_o)$ is decided by the relative magnitude of t_{ox} and γ where γ is constant factor which functionally relates the σ_{ox} and the potentials as follows:

$$\log(\sigma_{ox}) \approx \gamma \log [(\phi_G-\phi_S-\phi)/(t_{ox}+d)] \tag{21}$$

and $f_2/f_1 \approx -\gamma/t_{ox}$.

Therefore,

$$\sigma_J^2 = (\sigma_{ox}/t_{ox}LW)^2(\sigma_o^2\ 2\pi\beta^2(\psi_G-\psi_S)^2\gamma^2/t_{ox}{}^2) \int_S \int dS$$

$$= (\sigma_{ox}/t_{ox}LW)^2(\sigma_o^2\ 2\pi\beta^2(\psi_G-\psi_S)^2\gamma^2 LW/t_{ox}{}^2) \quad . \tag{22}$$

The relative rms deviation is

$$R_2 = \sqrt{\langle J_1^2 \rangle}/J_o = \sigma_o \sqrt{2\pi}\beta\gamma/t_{ox}\sqrt{LW} \qquad (23)$$

Hence

$$SF_{P2} = \sqrt{2k_1}\ (1+R_2) \quad . \qquad (24)$$

RESULTS

Presently three major overstressing aspects are considered: 1) The first one refers to unperturbed geometry of a MOS structure and the overextending influence of the geometry and material of the field-plate is quantified via the parameter k_1. For a given gate-oxide, the severity is then specified by SF_U being directly proportional to the width W and is inversely proportional to $\sqrt{t_f \sigma_f}$. That is, the thinner field-plates of less conductive material(s) would significantly enhance the overstressings. For typical values of L ≃ 100 μm, t_{ox} ≃ 500 Å, t_f ≃ 2000 Å and $\sigma_{ox} \simeq \sigma_{si}$ (under post-breakdown conditions), severity with metallic electrodes (such as W, Mo, Al) is only about 10% relative to the severity with a polysilicon electrode. Under similar conditions $MoSi_2$ field-plate will pose about 31.5% of threat relative to the conditions with a polysilicon electrode. If the thickness of the

field-plate is very large, the factor SF_U will tend to be unity via (3). 2) The second consideration addresses the influence of stochastical perturbations in the rectangular boundary of the gate-oxide region; the corresponding overstressing is expressed by a factor R_1 so that the overall severity is quantified through SF_{P1} given by (13). Relative to an unperturbed structure, severity is essentially decided by R_1. Therefore, by dimensional scaling-down, say, when all the physical dimensions are multiplied by a factor, $\theta < 1$, R_1 becomes approximately equal to $1/\sqrt{\theta^3}$. That is, by scaling-down a MOS structure by a factor $\theta = 0.2$ (say), the severity due to edge-perturbations will increase by a magnitude equal to 11. 3) The third aspect of overstressing arises from the random variations in the gate-oxide. Again, relative to an unperturbed structure, severity is decided by the term R_2 of (24). If all physical dimensions are multiplied by the scaling factor $\theta<1$, the value of R_2 is close to $1/\theta^2$. That is, for a scaling factor of $\theta = 0.2$ (say), severity due to stochastical variations in the gate-oxide thicknesses will be 25 times larger. However, if t_{ox} is left unchanged and only the area (LxW) is scaled down, then R_1 is nearly equal to $1/\theta$, so that with $\theta = 0.2$, $R_1 \simeq 5$; it means that only a smaller influence on the severity can be expected [13].

Thus the thin-oxide breakdown in MOS structure is significantly influenced not only by the dielectric integrity, but also by the geometrical and material

characteristics of field plates. In addition, the stochastical variations or perturbations at the edges and the thickness of the gate-oxide will also profusely enhance the overstressing severity. Especially, when scaling down strategies are attempted, care should be taken to minimize the perturbation level, lest failures due to dielectric breakdown will be augmented. The breakdown characteristics of thin dielectrics with stochastical edge/thickness can also be analyzed by applying perturbation technique to the integral equation formulations due to Olsen [14]. Attempts are being pursued to obtain relevant closed form solutions.

ACKNOWLEDGEMENTS

This work was supported by Office of Naval Research (ONR Contract #613-005) which is gratefully acknowledged.

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CAPTIONS FOR THE DIAGRAMS

Fig. 1 MOS structure with unperturbed gate-region

Fig. 2 MOS structure with a gate-region having a stochastic edge

Fig. 3 Perturbed boundry: Enlarged view

Fig. 4 MOS structure with a stochastical gate-oxide thickness

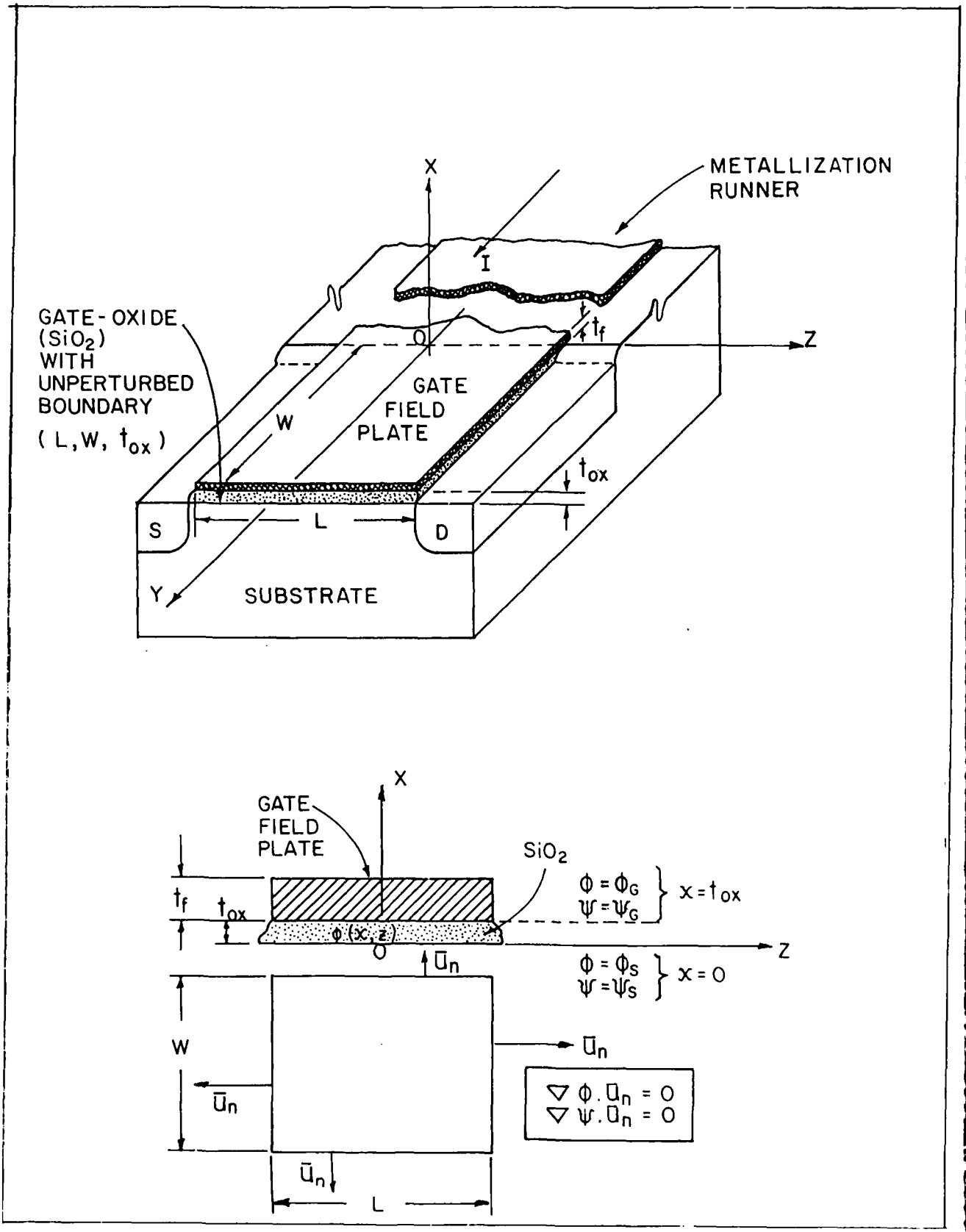

X
METALLIZATION
RUNNER
I
GATE - OXIDE
(SiO_2)
WITH
UNPERTURBED
BOUNDARY
(L, W, t_{ox})
t_f
Z
GATE
FIELD
PLATE
W
t_{ox}
S
L
D
Y
SUBSTRATE
X
GATE
FIELD
PLATE
SiO_2
$\phi = \phi_G$
$\psi = \psi_G$
$x = t_{ox}$
t_f
t_{ox}
$\phi(x, z)$
Z
$\bar{U}_n$
$\phi = \phi_S$
$\psi = \psi_S$
$x = 0$
W
$\bar{U}_n$
$\bar{U}_n$
$\nabla\phi \cdot \bar{U}_n = 0$
$\nabla\psi \cdot \bar{U}_n = 0$
$\bar{U}_n$
L

Fig. 1

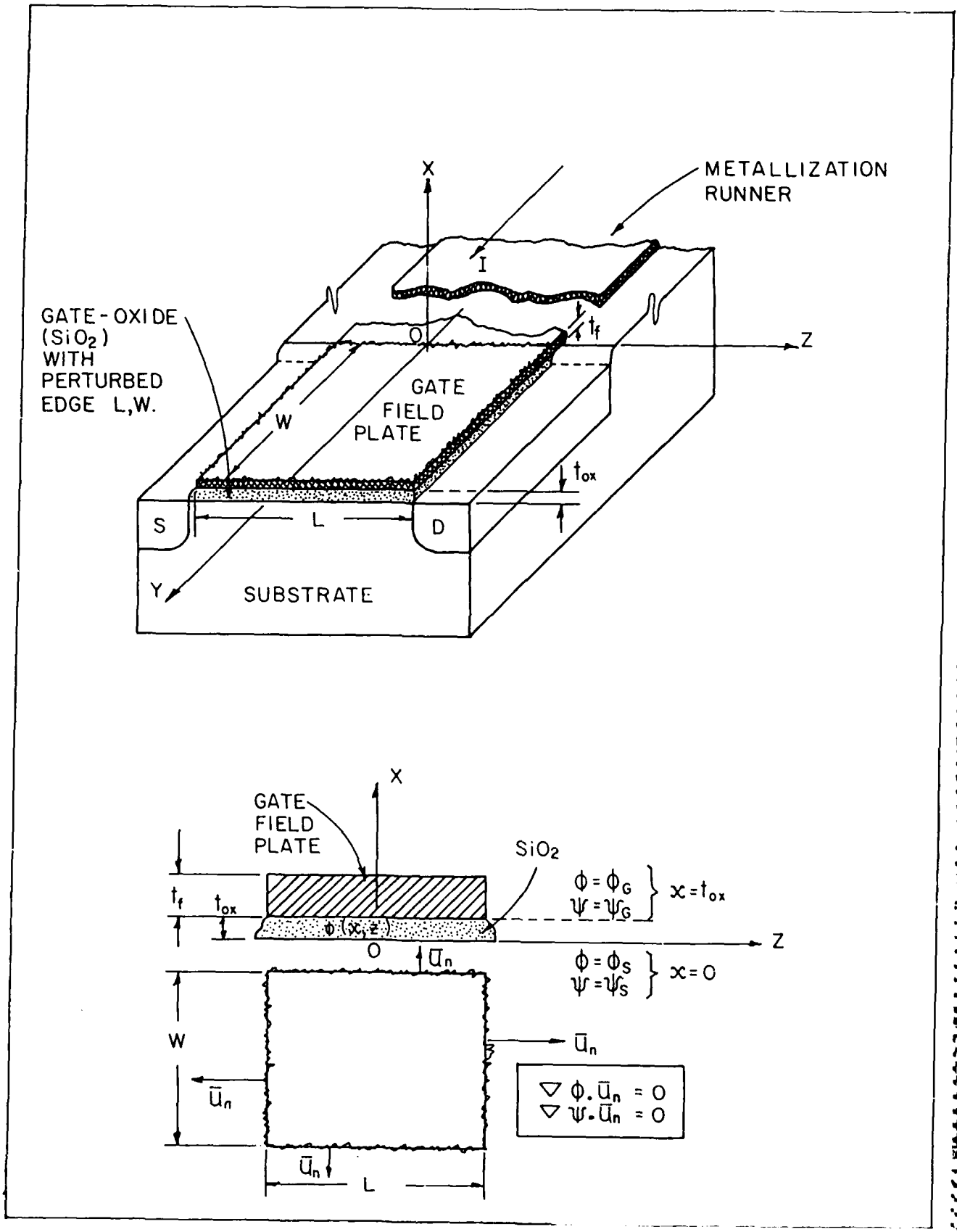

X
METALLIZATION
RUNNER
I
GATE - OXIDE
(SiO_2)
WITH
PERTURBED
EDGE L,W.
O
t_f
Z
W
GATE
FIELD
PLATE
t_{ox}
S
L
D
Y
SUBSTRATE
X
GATE
FIELD
PLATE
SiO_2
$\phi = \phi_G$
$\psi = \psi_G$
$x = t_{ox}$
t_f
t_{ox}
$\phi(x, z)$
Z
O
$\bar{u}_n$
$\phi = \phi_S$
$\psi = \psi_S$
$x = 0$
W
$\bar{u}_n$
$\bar{u}_n$
$\nabla\phi \cdot \bar{u}_n = 0$
$\nabla\psi \cdot \bar{u}_n = 0$
$\bar{u}_n$
L

Fig. 2

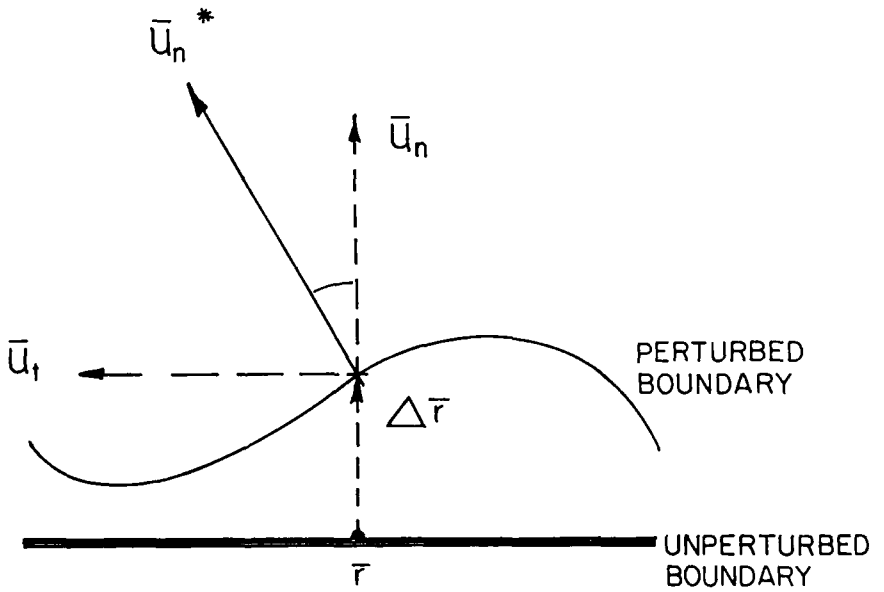

$\bar{u}_n^*$
$\bar{u}_n$
$\bar{u}_t$
PERTURBED
BOUNDARY
$\Delta\bar{r}$
UNPERTURBED
BOUNDARY
$\bar{r}$

Fig. 3

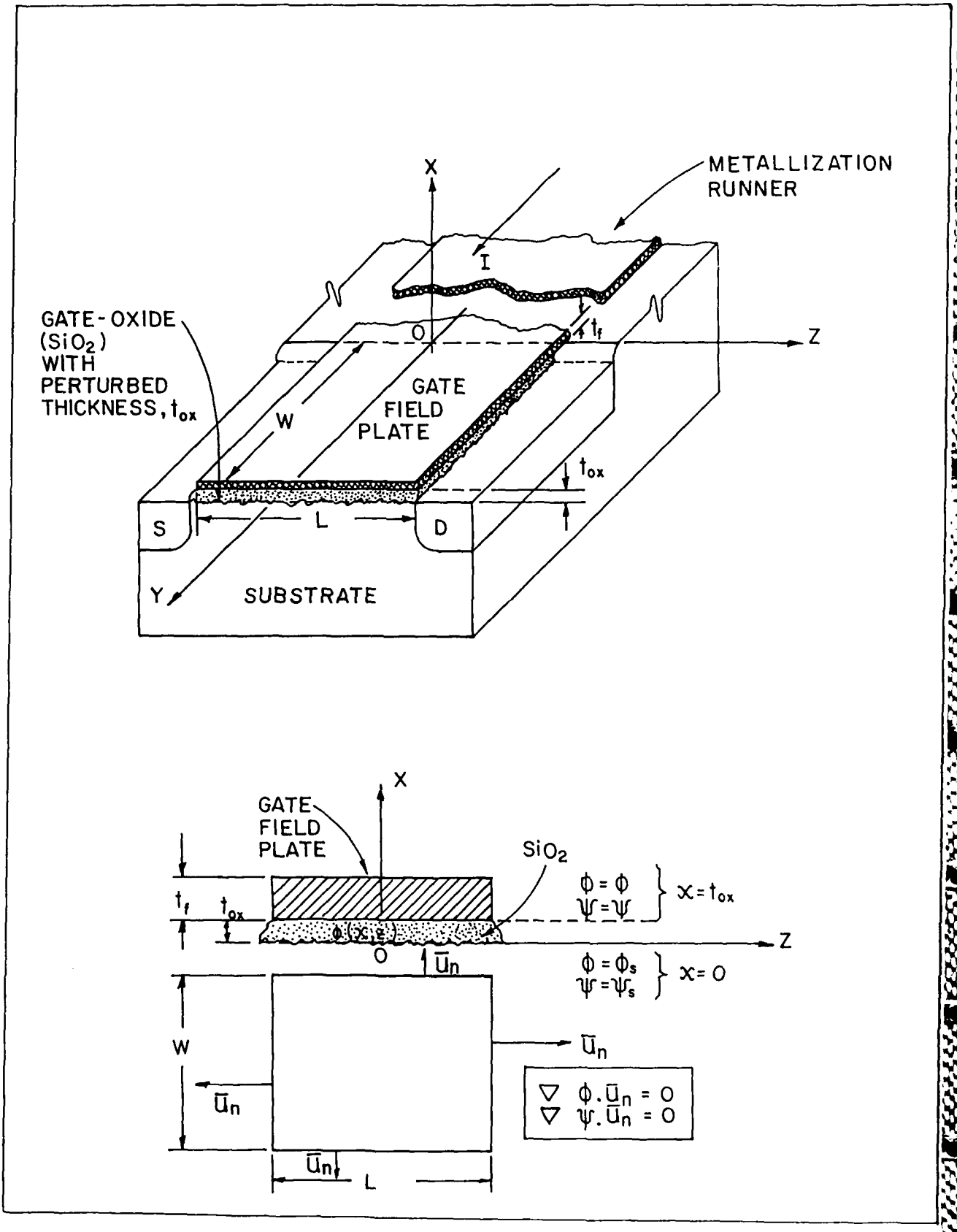

X
METALLIZATION RUNNER
I
GATE-OXIDE (SiO_2) WITH PERTURBED THICKNESS, t_{ox}
O
t_f
Z
W
GATE FIELD PLATE
t_{ox}
S
L
D
Y
SUBSTRATE
X
GATE FIELD PLATE
SiO_2
$\phi = \phi$
$\psi = \psi$
$x = t_{ox}$
t_f
t_{ox}
Z
O
$\bar{u}_n$
$\phi = \phi_s$
$\psi = \psi_s$
$x = 0$
W
$\bar{u}_n$
$\bar{u}_n$
$\nabla \phi . \bar{u}_n = 0$
$\nabla \psi . \bar{u}_n = 0$
$\bar{u}_n$
L

Fig. 4

NOTE

VOLTAGE BREAKDOWN IN MOS CAPACITORS: OVERSTRESSING SEVERITY DUE TO THE GEOMETRY AND MATERIAL OF THE FIELD-PLATE

High reliability performance [1-4] with ultra-density packaging warrants a thorough understanding of the physics of thin-oxide breakdown in MOS structures under high stress conditions. In the existing practice, simulation studies are carried out with tailor-made test samples formed by Al, Mo, Wo, polysilicon or silicide field-plate(s) of circular or rectangular geometry, with p or n type material being the substrate of the test structures [5]. Relevant studies address the influence of oxide-thickness, crystal purity/contamination, dielectric integrity and processing methods on the breakdown characteristics. Further, the overstressing effects of applied voltage parameters, namely, amplitude, polarity, transient waveform artifacts, continuous or pulsed excitation, duty cycle, etc., on the thin-oxide have also been broadly analyzed [6]. However, the effects of material and geometry of the field-plate have not been seriously considered in depicting the overstressings in MOS capacitors, except for the collection of some experimental data from post-breakdown examinations [7] which reveal that about 80% of failure sites cluster at the corners (of rectangular/square field-plate(s) and the reminder at the edges of the plate); some qualitative explanation based on electric field concentration

at the field-plate corners has been presented to justify these observed results. Thus, from the available studies it is clear that for a given stressing voltage, the breakdown of oxide-dielectric is determined not only by the intrinsic dielectric integrity of the oxide but also by the extrinsic (overstressing) influence of the geometry and the material of the field-plate.

Rigorous analytical formulations which exclusively assess the effects of field-plate geometry and its material in terms of post-breakdown voltage and current distributions beneath the field-plate are developed here. That is, post-breakdown current distribution is considered as an implicit indicator of overstressing influence or severity due to the field-plate parameters. Relevant results will indicate the extent to which the breakdown will be affected by the finite-sized field-plate (of finite electrical conductivity) in relation to an ideal system wherein the field-plate influence is presumed to be absent so that the breakdown is entirely determined by the oxide thickness and its integrity.

RECTANGULAR FIELD-PLATE MOS CAPACITOR

Fig. 1a depicts the geometry to be analyzed. A rectangular disk (field-plate) is separated by a thin oxide-dielectric from a semi-infinite substrate. Should the breakdown due to an applied voltage ϕ_o occur, the potential (ϕ) distribution below the field-plate can be determined by solving the differential equation with appropriate boundary conditions.

Thus, referring to Fig. 1a, the injected current, upon breakdown, is assumed to be evenly distributed over the width (B) of the plate and flows in the y-direction down the field-plate from the runner metallization along the length L. Considering, the y-directed current flows in the field-plate and in the substrate-sheath below the gate-dielectric, the differential equation for the post-breakdown potential distribution ϕ below the field-plate can be deduced from the following relations: 1) Over the differential length dy, the current $dI_y = (\sigma_{ox}/t_{ox})\, B\phi dy$; and $I_y = Bt_f\sigma_f E_y$ where E_y is the electric field gradient along y; further, 2) current continuity relation, namely, dI_y (field-plate) + dI_y (substrate-sheath) equal to zero is satisfied. Here σ_{ox} and t_{ox} depict the post-breakdown oxide conductivity and the gate-oxide thickness, respectively. Likewise σ_f and t_f represent the electrical conductivity and the thickness of the field-plate, respectively. Hence, with a dimensionless constant Y=y/L, the potential distribution (ϕ) can be specified by,

$$d^2\phi/dY^2 = 2k_1\phi \tag{1}$$

where $k_1 = \sigma_{ox} L^2/t_{ox}t_f\sigma_f$. Eqn. (1) can be solved with the boundary conditions, namely, $\phi = \phi_o$ at Y=0 and $d\phi/dY=0$ at Y=1. The result is,

$$\phi = A \exp(\sqrt{2k_1}\, Y) + B \exp(-\sqrt{2k_1}\, Y) \tag{2}$$

where

$A = \phi_o/[\exp(2\sqrt{2k_1})-1]$ and

$B = \phi_o \exp[2\sqrt{2k_1}] / [\exp(2\sqrt{2k_1})-1]$.

CIRCULAR FIELD-PLATE MOS CAPACITOR

Relevant to the circular field-plate geometry of Fig. 1b, the governing differential equation describing post-breakdown potential distribution in the dielectric (gate-oxide) region is given by

$$d^2\phi/dR^2 + (1/R)d\phi/dR = 2k_2\phi \qquad (3)$$

where $R = r/a_f$, $k_2 = \sigma_{ox}a_f^2/t_{ox}t_f\sigma_f$ and a_f is the field-plate radius. Assuming that the electrical contact at the centre of the field-plate has a diameter $2a_c$ over which current is injected evenly (during the post-breakdown situation), solution to eqn. 3 can be written in terms of Bessel functions as (I_n and K_n, n = 0,1,2...) as [8]

$$\phi = CI_o(\sqrt{2k_2}R) + DK_o(\sqrt{2k_2}R) \qquad (4)$$

distinguishability between the breakdown due to the failure in dielectric integrity and that caused by field-plate induced, nonuniform electric-flux concentrations. Thus, the severity of electrical overstressing due to uneven current or potential distribution caused by the finite thickness and conductivity of the field plate can be expressed as the ratio $SF = I_U/I_A$ where I_U denotes the current that would flow if the current density was uniform and equal to the maximum observed; and I_A is the actual total current fed to the field-plate. For the rectangular geometry (Fig. 1a), it can be shown that

$$SF_R = \sqrt{2k}_1/\tanh \sqrt{2k}_1 \tag{6}$$

and for the circular geometry (Fig. 1b),

$$SF_C = \left[\frac{2}{p}\,\frac{a_c a_f}{(a_c^2-a_f^2)}\,\frac{CI_1(q)-DK_1(q)}{CI_o(q)+BK_o(q)} + \frac{a_c^2}{a_f^2}\right]^{-1} \tag{7}$$

RESULTS & DISCUSSION

In practical devices, the field-plate materials used [5] are Al, polysilicon, silicides/polycides, (such as $MoSi_2$), W, Mo, etc. From eqns. (6) and (7) it is clear that for a given gate-geometry/dimensions, the severity is decided by the electrical conductivity of such field-plate

materials. For a typical gate structure with rectangular field-plate, the practical value of k_1 will be large and therefore severity expression of eqn. (6) reduces to (via large argument approximation)

$$SF_R \simeq \sqrt{2k_1} \quad . \tag{8a}$$

Likewise, for the circular geometry with $a_c/a_f \ll 1$ and $k_2 \gg 1$, eqn. (7) simplifies to [8]

$$SF_C \simeq \sqrt{2k_2} \quad . \tag{8b}$$

Table 1 illustrates the relative severity due to identical field-plates (of rectangular geometry) but of different electrical resistivities. The results show how the electrode resistivity of the gate-electrode would play a significant role in deciding the severity of breakdown. Further, if a circular geometry is used with the gate electrode covering the oxide over the same area as a square field-plate (that is, $L^2 \simeq \pi a_f^2$), from eqn. (8), it can be deduced that the severity involved in the case of circular structure will be enhanced by a factor of $\sqrt{\pi}$, assuming the gate-material in each being the same.

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CAPTIONS FOR THE DIAGRAMS

Fig. 1a MOS CAPACITOR WITH RECTANGULAR FIELD-PLATE GEOMETRY

Fig. 1b MOS CAPACITOR WITH CIRCULAR FIELD-PLATE GEOMETRY

Table 1. Relative Severity Factors

Data	Rectangular Gate-Electrode Structure			Equal-Area Circular Gate-Electrode Structure
	$L = 100\mu m$ $t_{ox} = 500$ Å $t_f = 2000$ Å $\rho_{ox} = 1/\sigma_{ox} = 1/\sigma_{Si}$ (Under Post-Breakdown Conditions)			$\pi a_f^2 = L^2$
Material	Electrical Resistivity ρ in ohm-cm	k_1 (Dimensionless)	Relative Severity (Rectangular Geometry) SF (Test Material) / SF (Silicon)	Relative Severity (Circular Geometry)
1) W, Mo, Al	$\approx 10^{-5}$	1×10^4	0.100 (10%)	0.177 (17.7%)
2) $MoSi_2$	$\approx 10^{-4}$	1×10^5	0.316 (31.6%)	0.558 (55.8%)
3) Si	$\approx 10^{-3}$	1×10^6	1.000 (100%)	1.772 (177.2%)

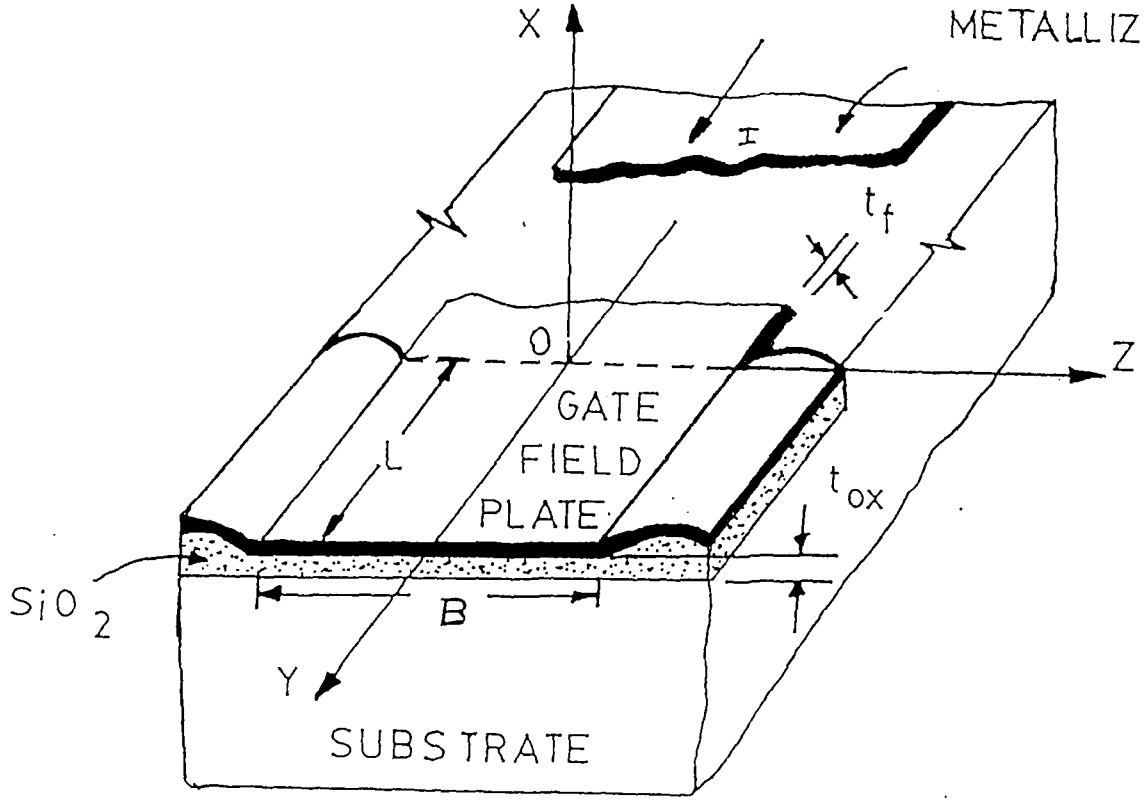

X
METALLIZATION RUNNER
I
t_f
0
Z
GATE
FIELD
PLATE
L
t_{ox}
SiO_2
B
Y
SUBSTRATE

FIG. 1a

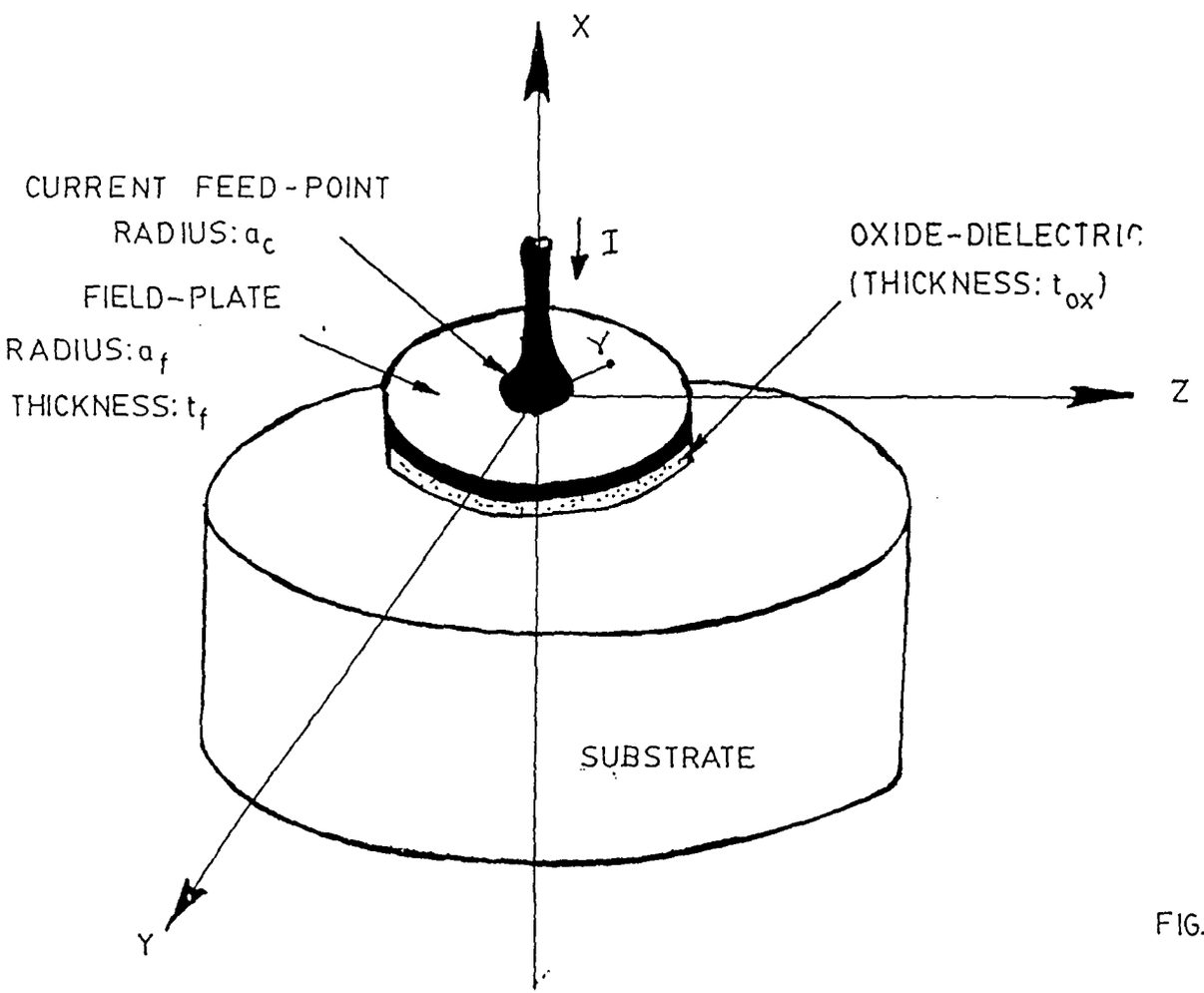

X
CURRENT FEED-POINT
RADIUS: a_c
FIELD-PLATE
RADIUS: a_f
THICKNESS: t_f
I
OXIDE-DIELECTRIC
(THICKNESS: t_{ox})
Y
Z
SUBSTRATE
Y

FIG. 1b

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6. PERFORMING ORG. REPORT NUMBER	
7. AUTHOR(s): Dr. Ibrahim R. Turkman, Dr. P. S. Neelakantaswamy	8. CONTRACT OR GRANT NUMBER(s): N00014-84-K-05
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18. SUPPLEMENTARY NOTES

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A Novel On-Chip Protection Method which uses a Vertical Static Induction Transistor underneath each bonding pad to sink the ESD current directly to the substrate

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A NOVEL ON-CHIP ESD PROTECTION DEVICE USING STATIC INDUCTION TRANSISTOR PRINCIPLE

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Abstract

Existing on-chip protection networks include one or several pn-junctions as static discharge by-pass paths. The high field and/or current crowding regions associated with the pn-junctions increase significantly the vulnerability of protection networks to ESD damage. Presently a novel on-chip protection method which allows the sinking of discharge current directly from the pad to the substrate by implementing a vertical static induction transistor underneath each bonding pad is described. This design avoids lateral flow of discharge current on the chip-surface, removes any reverse-biased junction along discharge path, saves the chip area by rendering the possibility of being implemented under the contact pads and offers the advantages of high speed and good thermal stability by virtue of being a majority-carrier device.

I. Introduction

Although considerable progress has been made in the design and implementation of on-chip static protection networks, they still remain prone to premature failure(s). The main reason for such vulnerability of these networks is that they are all based on a combination of resistors, diodes, transistors and/or four layer devices and that consequently, they include one or several pn-junctions along the static discharge path. Essentially non-uniform heat dissipation at the periphery of diffused regions in the reverse-biased junctions, is the most commonly observed cause of failure as reported in the literature [1][2][3][4]. Even the thick-field-oxide transistor which is currently considered to be the most effective for NMOS and CMOS protection (Fig. 1a), suffers from excessive localized heating at its reverse-biased drain-to-substrate junction.

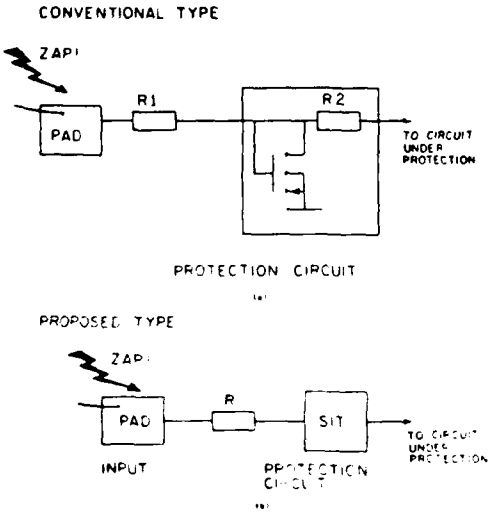


FIG. 1: ON-CHIP PROTECTION METHODS

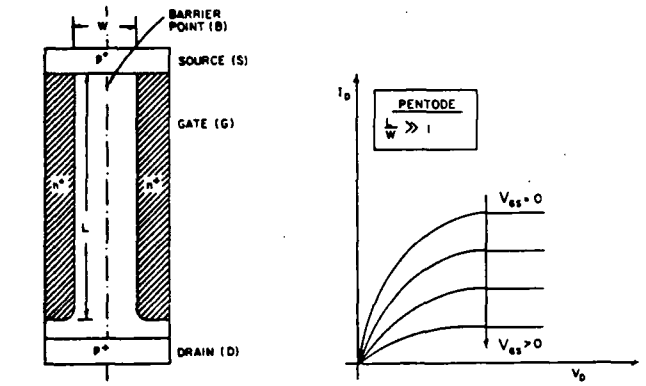
Excessive temperature rise at the drain region of stressed thick-oxide NMOS FETs has been observed by using infrared microscopy technique [4]. Further, scanning electron micrographs of damaged thick oxide protection devices show that the device failures are due to the formation of metal/silicon shorts between the drain contact and the channel and/or the bulk of the substrate as a result of electrothermal migration [1]. The temperature rise may even be so large as to cause polysilicon filament formation shorting the polysilicon from the gate to the drain and sometimes to the source regions as observed in output buffer FETs damaged by ESD transients [1].

Such localized heating stems from the presence of intense field and/or current regions in the pn-junctions. The power dissipation level and hence the resulting damage are more pronounced when the junction is reverse biased explaining why the drain region is the prime damage site. These high field and/or current crowding regions are inherent to pn-junctions, not only because the total elimination of structural and layout irregularities in practice is impossible, but more specifically because of the existence of curved peripheral junction regions in the planar technology. Furthermore, the thick-oxide protection devices are designed to operate in the so-called snap-back or bipolar second breakdown mode in order to clamp the ESD voltage transient to values low enough to cause no damage to the protected internal gate oxides [5]. The two other possible modes of conduction for these devices, namely, the MOS transistor mode and the punch through mode, correspond to an unacceptably large on-resistance and therefore will be totally inadequate for the protection of future submicron geometry MOSFETs with gate dielectric thicknesses ranging from 100 to 300 A. On the other hand, it is well known that the possibilities of thermal runaway, current filamentation and subsequent device failure are greatly increased when a semiconductor device is forced to operate in the second breakdown mode. In summary, it appears that a substantial improvement in the performance of on-chip protection networks would be possible by designing them in a way that no reverse-biased pn-junction operating under the first and especially the second breakdown conditions is present along the intended static discharge path. Moreover, the designers should take advantage of continuous increase in the use of thin epitaxial layers in NMOS and CMOS technologies which makes it possible to sink the static current to the substrate through a low impedance path instead of allowing it to flow laterally at the surface of the chip. In the following sections a vertical static induction transistor (SIT) structure is proposed and discussed as an attractive way of implementing the above mentioned design considerations (Fig. 1b).

II Static Induction Transistor as an ESD Protection Element

The Static Induction Transistor (SIT) has been introduced by Nishizawa, et al. [6], as a solid state

device with characteristics similar to the vacuum tube triode. Its both output and input characteristics are based on the static induction principle [6]. It is basically a short-channel JFET which, unlike the usual saturating pentode-like I-V characteristics of JFETs, presents triode-like I-V characteristics (Fig. 2 and 3).



CONVENTIONAL JFET

PENTODE-LIKE IV CHARACTERISTICS

FIG. 2: CONVENTIONAL JFET

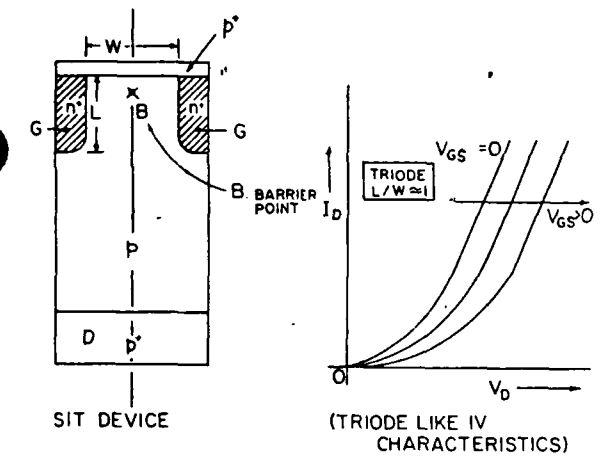


FIG. 3: STATIC-INDUCTION TRANSISTOR

Triode-like behavior arises from the proximity of source and drain regions and the ability to modulate the electrostatically induced potential barrier at the source-end of the channel, not only by the gate voltage (as in standard JFETs), but also by the drain voltage. This requires the product $(r_s \cdot g_m)$ to be much less than unity. (Here r_s denotes the differential channel series resistance after pinchoff and g_m is the device transconductance.) In practice this condition is established by making the channel length L comparable to its width W; hence the term "short-channel" is used above.

The major mechanism of current transport in SIT is majority carrier injection over the source-to-channel potential barrier. The device is known for its low impedance, high current density capability (several 1000A/cm^2), good thermal stability, high transconductance and fast response time (in the order of a nanosecond). Hitherto SITs have been realized as power microvave devices (100 W output power at GHz frequencies) [7][8][9][10], high power-high frequency transistors (few KW at MHz frequencies) [6], high (breakdown) voltage power devices [11] as well as VLSI level logic circuit elements (SIT-I^{2}L) [12].

The high current-high speed properties of SIT makes it also suitable as an on-chip ESD protection element. The device proposed here is a vertical, normally OFF type SIT that operates under $V_{GS}= 0$, with the channel being depleted and the source potential barrier being established by the built-in potential of the gate to source junctions. The structure can be incorporated directly under the contact pad areas. For a chip using a p-type epitaxial layer on p+ substrate, the relevant processing steps can be summarized as follows (Fig. 4):

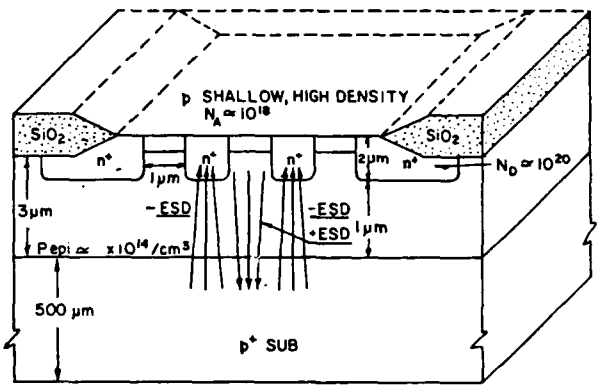


FIG. 4: PROPOSED ON-CHIP PROTECTION SCHEME USING SIT PRINCIPLE

a) Unlike the standard practice of having the bonding pads on the field-oxide, the oxide is removed from the pad locations. This could be, for instance, a part of a LOCOS process scheme with the provision that all subsequently deposited thin films prior to metallization should be selectively removed from the pad areas.

b) An n^+ grid (gate) is formed by lithographic means and doping/annealing techniques. The distance between adjacent n^+ diffused regions (channel width W) should be small enough to deplete the vertically sandwiched p-layer (the channel) under equilibrium conditions. Typically, a channel which is about a micron wide and doped in the mid-10^{14}/cm^3 range would be totally depleted.

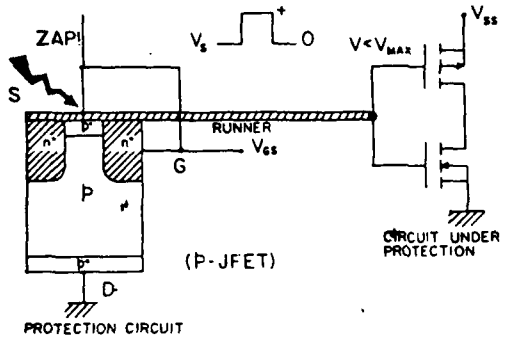
c) A blanket shallow p^+ doping (source) is introduced at the surface of the p-epi layer. This p^+ layer serves a dual purpose: first it prevents the high electric fields that are generated within the channel region from reaching the silicon surface; and secondly, it introduces a p^+p high-low junction which increases the channel barrier height and thus reduces the pad to substrate leakage current under normal operating conditions, (that is, without an ESD event).

d) Aluminum is deposited and left over the entire pad area(s). If the p^+ doping level is below the surface

doping density of n^+ fingers, the pad metallization introduces a short between the top source and gate fingers, and the resulting device may be called a surface grid SIT. Otherwise, a buried n^+ grid version is also possible as long as the pad metal covering the p^+ layer makes contact with the n+ grid at some point.

The p^+ substrate plays the role of drain region in this vertical structure. The ESD reliability may also be further enhanced by introducing p^+ polysilicon tabs between the pad metal and the p^+ source layers, in which case, the device is necessarily of the buried grid type. It is also possible to use the p^+ poly tab as the diffusion source for the formation of the p^+ source region in a way similar to the buried contact process technique.

To illustrate the operation of this protection device, consider a MOS circuit made on the p epi/p^+ substrate (Figure 5).



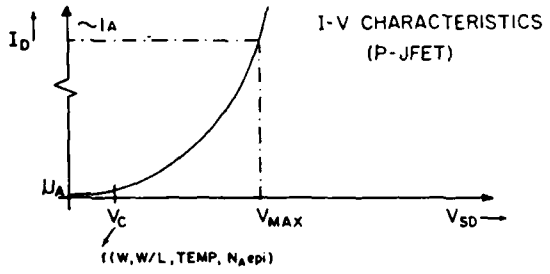


FIG. 5: OPERATION OF THE PROPOSED PROTECTION METHOD

For nominal voltage levels at the input pad (say 0 to 5V), the normally OFF SIT presents a large impedance path to the grounded substrate. The cut-in voltage V_C of the SIT, which is arbitrarily defined on Fig. 5 as the source-to-drain voltage V_{SD} corresponding to a uA drain current I_D for $V_{GS} = 0$ should be just above the positive nominal operating voltage. At the event of a positive polarity ESD, the increasing source-to-drain voltage results in the lovering of the source-to-channel potential barrier. The discharge current is sunk to the substrate through the multiple p^+-p-p^+ "channels" while the source, that is, the pad-voltage, is clamped to V_{MAX} which should be less than the dielectric breakdown voltage of the internal gate oxides. On the other hand, when a negative ESD occurs, the pad voltage is clamped by the then forward-biased pin-diode formed by the p^+ substrate, p-epi and n^+ grid regions. Although the static discharge current flows through a pn-junction like in the conventional protection networks, the device is expected to handle the relatively low power dissipation that is associatedwith forward biased diodes.

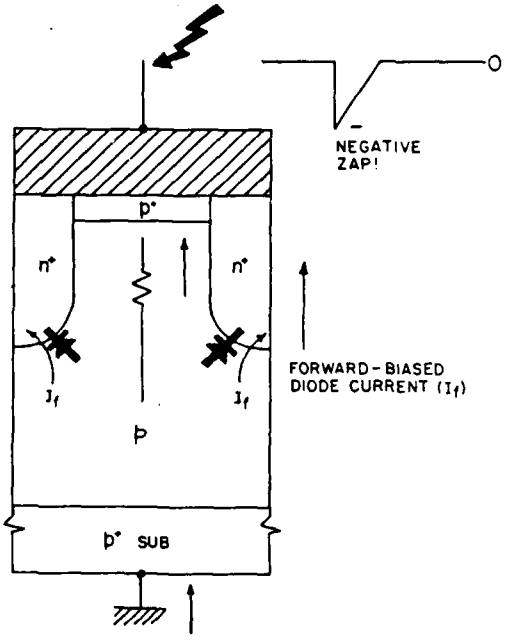


FIG. 6: PROTECTION UNDER NEGATIVE ZAPS

III. Design Considerations

Discussions in this section are subdivided into three parts: first, the OFF state characteristics of the SIT under normal IC operation conditions and the impact of the design parameters on these characteristics are analyzed; secondly, the behavior of the SIT at very high current densities that usually prevail during an ESD transient is examined; and finally a few remarks are made regarding the safe operation of the SIT at the event of a negative polarity ESD.

A. Off State Characteristics

The SIT should be designed to minimize the pad to substrate leakage current for nominal voltage values at the pad level. Under such low level injection conditions, the drain current I_D is approximately an exponential function of the source-to-drain voltage V_{SD} for $V_{GS} = 0$ (as well as for a given gate to source reverse bias). The key element in controlling I_D is the source-to-channel potential barrier ϕ_B over which the majority carriers are injected into the channel. ϕ_B varies across the channel width W, increasing towards the gate regions while presenting a minimum at the center of the channel. The drain current density J_D at given plane (x) across the channel width is exponentially dependent on the local barrier height $\phi_B(x)$, which in turn is a linear function of V_{SD}:

$$J_D(x) \propto \exp\left[-\left(\frac{\phi_B(x)}{KT/q}\right)\right] \propto \left[\exp - \left(\frac{a(x)\, V_{SD} + b(x)}{KT/q}\right)\right] \quad (1)$$

which upon integration leads to:

$$I_D \propto \left[\exp - \left(\frac{nV_{SD}}{KT/q}\right)\right] \quad (2)$$

The design related parameter n is positive and less than unity.

As ϕ_B plays the key role in determining the OFF state impedance of the SIT, the question is to find the range for ϕ_B which would be suitable for the present application. The use of SIT as a protection element requires a sub μA drain current in the absence of an ESD event. For an effective channel area $A = 10^{-4}$ cm^2 this would correspond to an average drain current density J_D of 10^{-2}A/cm^2 or less. A number of analytical, numerical and experimental studies have been carried out in the past to determine the dependency of I_D on V_{SD}, V_{GS} and various structural parameters such as the channel width W, length L and doping density N_{ch} [13][14][15]. Though these studies have largely focused on normally ON type SITs, bipolar mode SITs and/or SIT designs with no relevance to the results show that ϕ_B at the central plane of the channel should be greater than 650 mV if J_D is to be kept under 10^{-2}A/cm^2. In order to provide some design guidelines for the proposed protection element an analytical expression which, for $V_{GS} = 0$, gives the vertical potential distribution $\psi(z)$ along the central plane of the channel as a function of V_{SD} and structural parameters can be deduced [15]. It is given by

$$\psi(z_n) = \frac{16}{\pi^2} V_{SD} \sum_{\substack{m=1 \\ n=1}}^{\infty} \frac{\sinh[\pi(2n-1)(L/W)(1-Z_n)]}{(2m-1)(2n-1)\sinh[\pi(2n-1)(L/W)]} \times \sin\left[\frac{\pi(2m-1)}{2}\right] \cdot \sin\left[\frac{\pi(2n-1)}{2}\right]$$

$$+ \frac{32}{\pi^2} V_g \sum_{\substack{m=1 \\ n=1}}^{\infty} \frac{\sinh\left[\frac{\pi(2n-1)(W/L)}{2}\right]}{(2m-1)(2n-1)\sinh[\pi(2n-1)(W/L)]} \times \sin\left[\frac{\pi(2m-1)}{2}\right] \cdot \sin[\pi(2n-1)\, Z_n]$$

$$- \frac{64}{\pi^5} \frac{qN_{cb}}{\epsilon} \sum_{\substack{m=1 \\ n=1}}^{\infty} \frac{\sin\left[\frac{\pi(2l-1)}{2}\right] \cdot \sin\left[\frac{\pi(2m-1)}{2}\right]}{\left[\left(\frac{(2m-1)}{W}\right)^2 + \left(\frac{(2n-1)}{L}\right)^2\right]} \times \frac{\sin[\pi(2n-1)\, Z_n]}{[(2l-1).(2m-1).2n-1)]} \quad (3)$$

where $Z_n = z/L$ with $z = 0$ and $z = L$ representing the positions of the drain and source ends of the channel, respectively. Further, V_g denotes the n^+ gate to p^+source built-in potential. The constants q and ε have their usual meaning. This expression (eqn. 3) is based on the assumptions that the densities of the carriers within the channel are negligible compared to N_{ch} and that the length of the gate fingers is much larger than both W and L.

The effects of N_{ch}, W and L on the source to channel barrier height ϕ_B are summarized in Table 1. For each set of design parameters, ϕ_B is computed for V_{SD}= 0V (ϕ_{Bo}) and V_{SD} = 5V (ϕ_{B5}). V_g is taken as 1.1 V. These simulations show that for V_{SD} changing between 0 and 5V, channel doping density being less than 10^{15}/cm^3 and channel aspect ratio L/W of about 2 result in the desired range of the potential barrier, that is, ϕ_B>650 mV. Although it is possible to improve the barrier height and thus reduce the leakage current by increasing L/W beyond 2, such aspect ratios would cause the deviations in the triode like properties of the SIT.

Channel Doping \ Channel Dimension	W = 0.8 μm L = 1.5 μm	W = 1 μm L = 2 μm
$N_{ch} = 10^{14}$/cm^3	ϕ_{B0} = 912 mV ϕ_{B5} = 723 mV	ϕ_{B0} = 931 mV ϕ_{B5} = 774 mV
$N_{ch} = 5 \times 10^{14}$/cm^3	ϕ_{B0} = 870 mV ϕ_{B5} = 682 mV	ϕ_{B0} = 863 mV ϕ_{B5} = 709 mV
$N_{ch} = 10^{15}$/cm^3	ϕ_{B0} = 817 mV ϕ_{B5} = 632 mV	ϕ_{B0} = 779 mV ϕ_{B5} = 629 mV

Table 1 Potential Barrier Heights ($\phi_{BV,V=0,5}$): Design Values

B. Positive Polarity ESD Handling

At the event of a positive polarity ESD occurring, the pad voltage should be rapidly clamped to some tens of volts so as to avoid damage to the IC. For instance, since the dielectric strength of silicon dioxide is about 10MV/cm, the pad voltage should not exceed V_{SDmax} = 30V in the case of a 300 Å internal gate oxide technology. At such pad (or SIT source) voltages, the channel potential barrier vanishes and a very high level current-injection takes place, and as the density of majority carriers injected into the channel exceeds the channel doping density, SIT operates in the space-charge limited current flow mode. Assuming that the majority carriers (holes) move at their limiting velocity v_l (= 10^7 cm/s in Si), J_D and p are related through:

$$J_D = qpv_l \cdot \quad (4)$$

The injected-hole induced space charge generates a vertically oriented electric field within the channel and the portion of the epi layer which is between the channel and the p^+ substrate (drain). This electric field increases linearly from the p^+ source to the p^+ substrate with a slope given by:

$$\frac{dE}{dz} = \frac{q}{\epsilon} (p - N_{ch}) \quad (5)$$

Combining equations (4) and (5) and integrating $\varepsilon(z)$ from the p^+ source to the p^+ substrate with the assumption that the field at the source-channel high-low junction is much lower than elsewhere in the space-charge region, yields:

$$J_D = qv_1 \left(\frac{2V_{SD}\epsilon}{t^2 q} + N_{ch} \right) \quad (6)$$

where t is the total source to substrate distance which includes the channel length L. For V_{SDmax} = 30V, N_{ch} = 5 x $10^{14}/cm^3$ and t = 3μm, eqn. (6) predicts a J_D of approximately 7500 A/cm^2 which corresponds to an ESD current of 0.75A, if the effective channel area is set as 10^{-4} cm^2.

There are a number of important points which are pertinent to the above design/calculations:

1) The maximum field E_M in the SIT region occurs at the p epi - p^+ substrate junction. This peak field value should not approach the dielectric strength of silicon (300,000 v/cm approximately) at which point current-mode second-breakdown may occur as a result of a double-injection mechanism. E_M can be obtained by $(\frac{dE}{dx} \cdot t)$ which is equal to $\frac{2V_{SD}}{t}$ and is about 200,000 v/cm in the previous example.

2) Some spreading of the hole current is expected between the channel and the p^+ substrate.

3) The avalanche breakdown voltage of the parallel n^+ gate - p epi - p^+ substrate pin diode should be above the maximum expected pad voltage V_{SDmax}. The thickness (t-L) of the base of this pin diode should be designed larger than $V_{SD\ max}/3 \times 10^5$ v/cm) to prevent its breakdown. In the design example discussed, this condition can be satisfied by setting L = 1.5 μm which makes (t-L) = 1.5 μm.

Thus the results of this first order analysis suggest the current handling capability of SIT is appropriate for its use as an ESD protection device. It can certainly be improved by undertaking a more systematic device design, implementation, testing and optimization approach. It is also possible to implement the SIT in the proximity of the pad with a current limiting resistor as shown in Fig. 1b.

Negative Polarity ESD Handling

The negative polarity electrostatic zaps are handled by the pin diode path. In the case of a surface grid SIT, the metal to n^+ cathode contact is distributed over the entire pad area and is in close proximity to the n^+p junction at any device cross section. Consequently, no significant current crowding and intense local power dissipation should take place. However, if the structure is a buried grid SIT, the lateral flow of the ESD current along the narrow n^+ fingers could cause some local debiasing of the n^+p junction. Such nonuniformities in the current flow can be minimized by designing multiple contact regions between the pad metal and the buried grid.

IV Conclusions

1. The present work suggests the feasibility of using SIT as an on-chip ESD protection device.

2. The merits of such SIT based protection circuits are:
   a) It eliminates pn-junction(s) as against the conventional static bypass strategies.
   b) It allows the massive ESD current to sink vertically to the substrate.
   c) It is a majority carrier device with fast response time and good thermal stability.

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